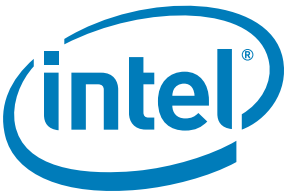

100BASE-TX/10BASE-T Physical Layer Compliance Tests Manual

June 2006

Version 1.0

Revision History

Date	Revision	Description
June 2006	4.30	Revised document with new Intel branding documentation templates.
May 2006	3.25	Updated Intel logo
June 2005	3.20	Replaced reference to the PhyConf tool with the LANConf tool.
Sept 2004	3.10	Revised Table 17-1 and Table 18-1. Both of these tables are related to PhyConf.exe configuration settings.
June 2003	3.00	Added information relating to 1000Base-T physical layer conformance.
May 2003	2.00	Added information for 10Base-T testing.
Jan 2003	1.15	Changed all references of ST.exe to PhyConf.exe.
Jan 2002	1.10	Removed ST.exe User Guide from appendices.
June 1998	1.00	First release.

Contents

1 Introduction

Networking is complex and involves a combination of advanced analog and digital technologies. To insure interoperability of networking solutions from various manufacturers, it is imperative that standard compliance testing is performed.

This document describes procedures for basic 1000Base-T, 100Base-TX, and 10Base-T American National Standards Institute (ANSI) Twisted Pair-Physical Medium Dependent (TP-PMD) physical layer, or PHY, conformance testing on Intel based networking solutions. It does not include the complete set of tests required for TP-PMD conformance. However, it does include a recommended subset of these tests. After completing the test procedures described in this manual, the tester should be able to identify and understand how to correct areas where the Unit Under Test (UUT) fails to conform to the ANSI X3.263-1995 standard.

The procedures in this document are not intended to be specific to a particular manufacturer's test equipment. Moreover, they do not encompass all methods that a test may be performed. The tester is assumed to have a basic knowledge of oscilloscopes, network analyzers, signal generators, etc. Advice for success in obtaining accurate measurements are included throughout the document in shaded boxes.

The test methods described in this document have been customized to test Intel networking silicon only. Results may vary if these procedures are used on other manufacturers' networking devices.

1.1 Basic Concepts

Recommended equipment settings are provided for each test procedure. These settings provide a good starting point for measurement. Different equipment may be able to provide better or worse resolution. Therefore, it is important to understand good triggering and display practices in order to obtain the best view of a waveform.

1.1.1 Calibration

Due to the precise measurements required for compliance testing, accurate measurement instruments are required. All equipment used during the testing process must be properly calibrated. Oscilloscopes must have a signal path compensation and probe calibration completed prior to testing.

1.1.2 Triggering

Determining the appropriate trigger point can mean the difference between passing and failing the ANSI TP-PMD physical layer conformance tests. For example, a signal that is wandering back and forth due to a bad trigger may cause enough jitter on the display to cause the UUT to fail (see Chapter 9). Triggering guidelines are provided throughout this document and provide a good starting point for measurement. Fine tuning adjustments may be necessary in order to achieve the best display.

1.1.2.1 Signal with an Ambiguous Trigger Level

An ambiguous trigger level (either width or height) can prevent a stable display.

1. Try to reduce the delta between the minimum and maximum pulse widths as much as possible.
2. Determine where the trigger level falls on the waveform.

If the line passes through more than one point on the rising edge of the waveform, raise or lower the trigger until a point is found that is unambiguous as illustrated in Figure 1-1.

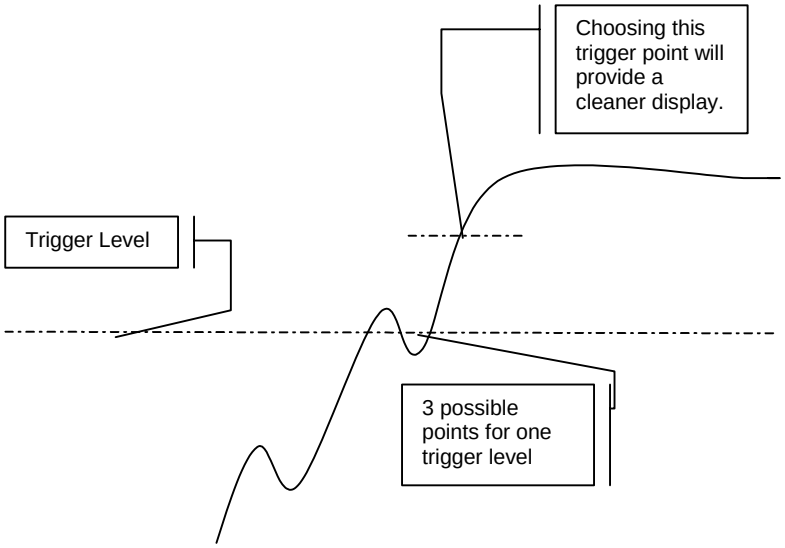

Figure 1-1. Ambiguous Trigger Level

1.1.2.2 Signal Does Not Appear

If the signal does not appear or appears only for an instant, the trigger level may be too high. Reducing the trigger level should cause the signal to appear (or re-appear).

1.2 Displaying Waveforms

When observing waveforms on the scope display, it is important to understand the purpose of the measurement being performed. If the purpose is simply to see a complete waveform, then the horizontal and vertical scales only need to be small enough to fit the waveform on the screen and the display does not need to be set to average or infinite persistence. However, if the purpose is to obtain the most accurate measurements, more care is needed. The recommended scope settings listed throughout the procedures should allow the desired waveform to be displayed on the screen. For the best resolution, zoom in as much as possible on the waveform as observed in the following three screen shots.

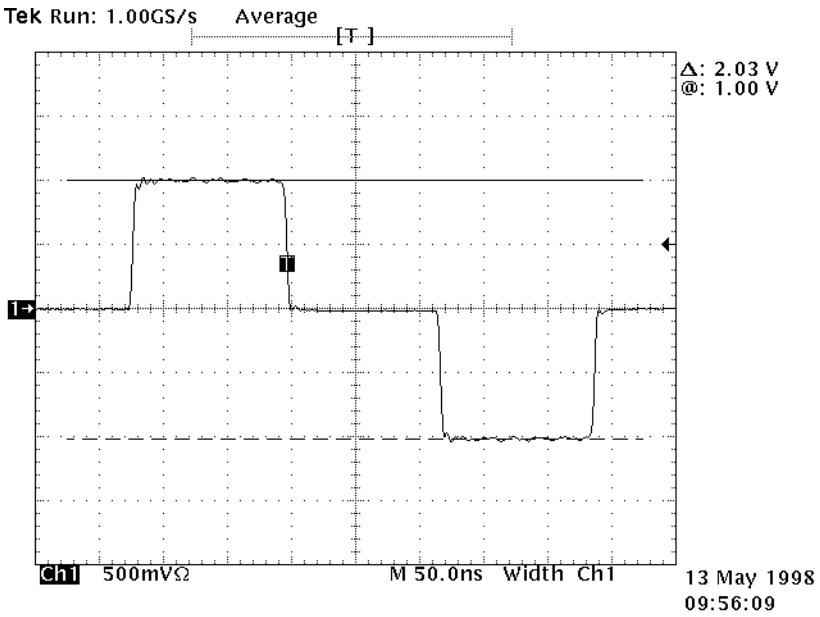

Figure 1-2. Poor Resolution (Wide View)

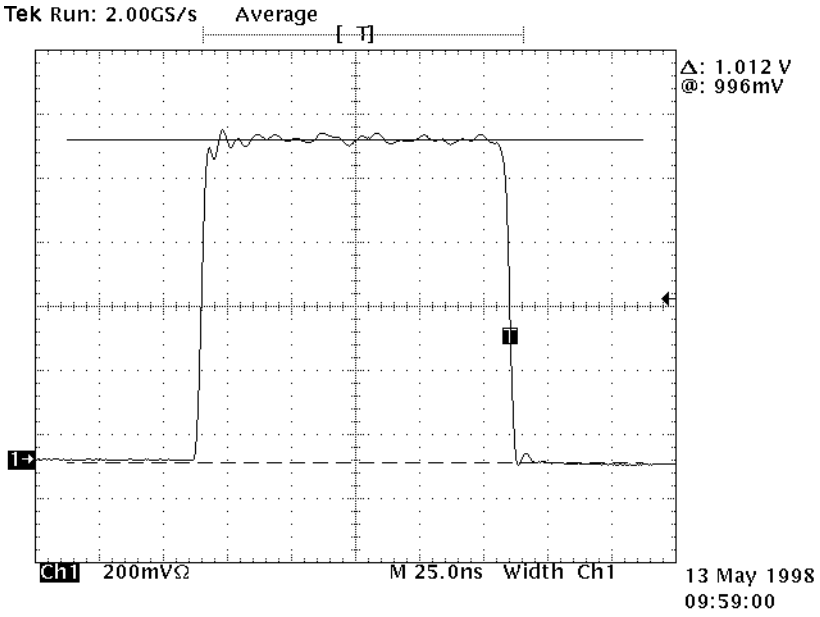

Figure 1-3. Good Resolution with Room for Improvement

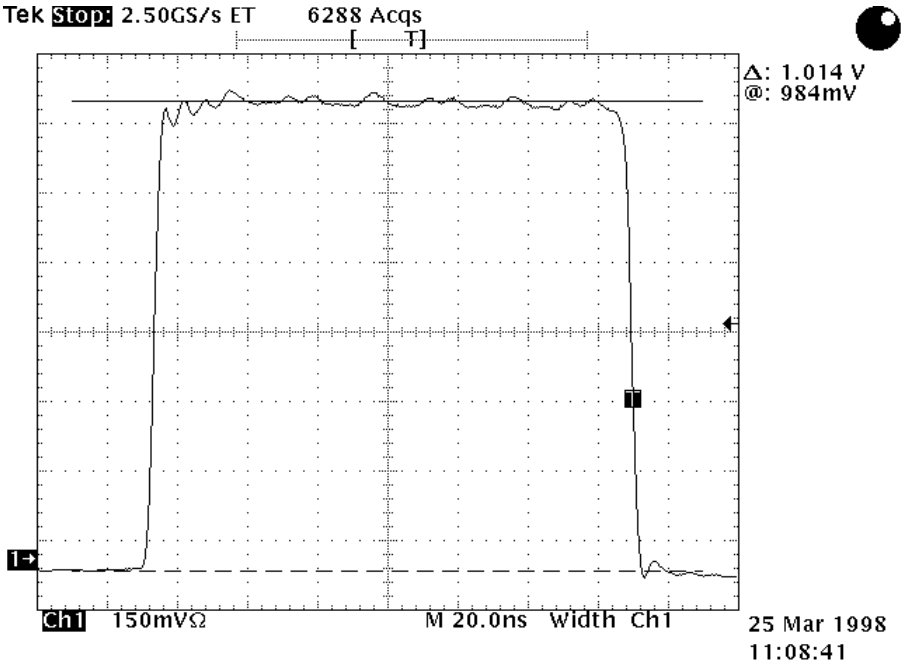

Figure 1-4. Best Resolution for Measurement

Note: The above three screen shots were not necessarily taken during the same session.

Note: The waveform in Figure 1-4 is displayed across the entire screen, showing enough of the edge of the pulse to allow the zero point to be approximated and providing the best resolution possible for measurement.

In the example above, the “Average” setting was used on the scope to produce a sharper image. This is the best (and easiest) way to measure the amplitude, period, overshoot, and rise/fall time of a waveform. Each time a new trigger signal arrives, the scope repaints the screen with a new signal. This causes the signal to appear unstable because each successive signal is not exactly the same as the previous one. By averaging the waveforms together, random noise will be filtered from the display, and a more representative signal will appear.

Some measurements require the scope display to be set to “Infinite Persistence” (specifically, Chapter 9). In this case it is important that each successive waveform falls within specified boundary conditions. In infinite persistence mode, an adequate sample is obtained from data accumulated between a one to ten minute time period.

1.3 Required Test Equipment

This section describes the minimum equipment needed to complete the test. A list of equipment that may meet these requirements is listed in Appendices A and B.

- Digitizing oscilloscope with at least 1 GHz bandwidth (or at least 100 MHz bandwidth for 10Base-T).
- Two high bandwidth differential probes (P6247) with capacitance less than or equal to 1 pF and a bandwidth greater than or equal to 1 GHz (or greater than or equal to

100 MHz for 10Base-T). Using lower bandwidth/higher capacitance probes may cause false failures of conformance tests.

- Current probe amplifier (if required).
- Link test pulse generator (LPTG).
- Host computer running LANConf.exe for 1000Base-T, 100 Base-TX or 10Base-T testing.
- Two computers with open PCI slots and GiConf.exe installed for 1000Base-T testing only.
- One Intel® 82543 controller-based 1000Base-T adapter to generate Ethernet traffic for 1000Base-T testing only.
- Network/spectrum analyzer (50 KHz to 500 MHz range).
- S-parameter or transmission/reflection test set.
- Sweep generator (1 V peak-to-peak sine wave, 100 KHz to 125 MHz).
  If a sweep generator is not available, a network analyzer may be used instead.

- Ammeter (must be able to measure as little as 1 mA).
- 6 V battery.
- BNC cable with 50-ohm impedance (approximately three feet long).
- BNC to hook clip.
- Three-inch Category 5 (CAT5) unshielded twisted pair (UTP) cable (CAT5 patch cable should not be used since it does not conform to CAT5 specifications).

Note: Disabling the link detect or using a link pulse generator allows 10Base-T ethernet to transmit without being connected to another ethernet device. If the test hardware has the ability to disable the UUT's receiver link detect, then an external LTPG is not required.

1.4 Test Fixtures

In order to complete the tests described in the ANSI TP-PMD standard, several test fixtures are needed. Most are built from standard, easy to find parts. However, there are some items that may need to be special ordered. For more information, see

1.5 Required Software and Data Patterns

Many of the tests in this procedure require the UUT to behave in a specified way. Intel's proprietary test utilities, LANConf.exe, allow the UUT to be configured into the desired state and to transmit and receive specific test patterns. Contact your local Intel sales office for more details and to obtain a copy of LANConf.exe.

1.6 PHY Conformance Tests

There are several different ways to group the tests in this procedure, depending on the intent of the tester. The minimum subset of tests necessary to catch the most problematic bugs in board design and implementation are listed in the following subsections.

1.6.1 Minimum Recommended 1000Base-T PHY Conformance Tests

40.6.1.2.1 Peak Differential Output Voltage and Level Accuracy

- 40.6.1.2.2 Maximum Output Droop
- 40.6.1.2.5 Transmitter Timing Jitter (Master and Slave Modes) - Unfiltered
- 40.6.1.3.2 Receiver Differential Input Signals (Receive Bit Error Rate)
- 40.8.3.1 MDI Return Loss
- 40.6.1.3.4 Alien Crosstalk Noise Rejection (Differential Noise Rejection)
- 40.8.3.3 MDI Common-Mode Output Voltage

1.6.2 Minimum Recommended 100Base-TX PHY Conformance Tests

- Chapter 2, “100Base-TX Differential Output Voltage (UTP)”
- Chapter 4, “100Base-TX Signal Amplitude Symmetry”
- Chapter 5, “100Base-TX Transmitter Return Loss”
- Chapter 6, “100Base-TX Rise and Fall Times”
- Chapter 8, “100Base-TX Duty Cycle Distortion (DCD)”
- Chapter 9, “100Base-TX Transmit Jitter”
- Chapter 10, “100Base-TX Differential Input Signals (BER)”
- Chapter 12, “100Base-TX Receiver Common Mode Rejection”

1.5.3 Minimum Recommended 10Base-T PHY Conformance Tests

- Chapter 13, “10Base-T Peak Differential Output Voltage on TD Circuit”
- Chapter 14, “10Base-T Harmonic Content”
- Chapter 15, “10Base-T TD Circuit Impedance (Transmitter Return Loss)”
- Chapter 16, “10Base-T TD Circuit Common-Mode Output Voltage”
- Chapter 17, “10Base-T Transmitter Output Timing Jitter with Cable Model”
- Chapter 18, “10Base-T Transmitter Output Timing Jitter without Cable Model”
- Chapter 19, “10Base-T RD Receiver Circuit Signal Acceptance Test (BER)”
- Chapter 20, “10Base-T RD Circuit Differential Input Impedance (Receiver Return Loss)”

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2 100Base-TX Differential Output Voltage (UTP)

ANSI SECTION 9.1.2.2

2.1 Test Purpose

To measure the peak differential output voltage, V_{OUT} at the transmit pins of the UTP connector (also known as the Active Output Interface or AOI).

2.2 Specification

For UTP, the differential output voltage, V_{OUT} , as defined in Specification 9.1.3 and Figure 2-1 shall be: 950 mV ≤ V_{OUT} ≤ 1050 mV.

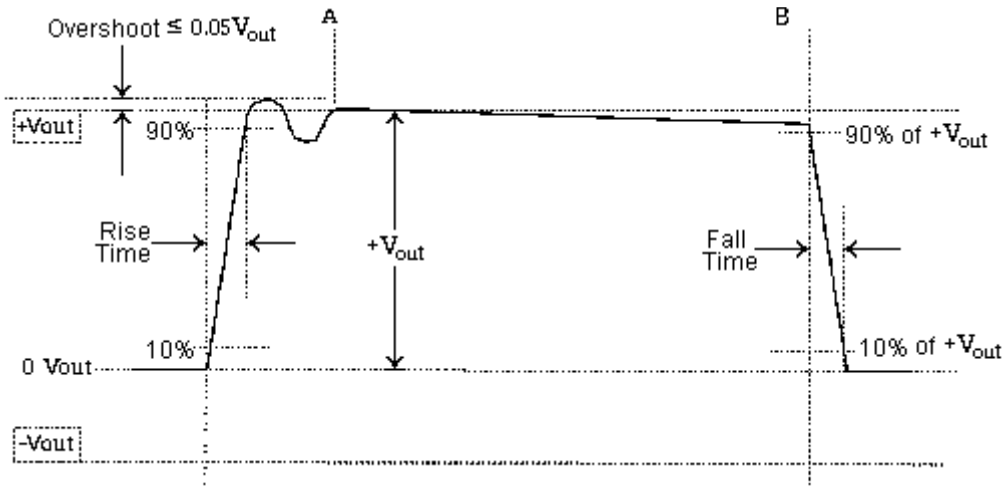

Figure 2-1. Waveform at Active Output Interface[1]

2.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

2.4 Test Fixtures

100 Ω UTP test load (Appendix D)

2.5 Test Procedure

1. Connect the test equipment and UUT as shown in Test Setup 1 in Appendix C.

1. Based on ANSI X3.263-1995, p 29, Figure 12.

2. Configure LANConf.exe as shown in Table 2-1.

Table 2-1. LANConf.exe Configuration for Differential Output Voltage (UTP)

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	66 bytes
8	Transmit Threshold	66 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable •

Table 2-2. Setting for Positive Differential Output Voltage (UTP)

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-150 mV to +1050 mV (1200 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

• Denotes LANConf.exe default setting.

3. Begin transmitting.
4. Configure the oscilloscope according to Table 2-2.

Table 2-3.)Setting for Negative Differential Output Voltage (UTP)

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-1125 mV to +75 mV (1200 mV over the full vertical scale)
Trigger Type	Negative pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	-500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 500 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 200 ns and the lower bound parameter to approximately 116 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

5. Select the horizontal cursors. Move one cursor to $+V_{OUT}$ and the other to 0.

Measuring Peak Voltages

When measuring positive and negative peak voltages, do not use the absolute values on the screen. Often it will appear as thought the start and finish of the MLT-3 waveform do not go through zero. This is caused by the oscilloscope or probes adding in a small DC offset. To record the correct peak values, run one horizontal cursor through the middle of the “zero” of the waveform as shown in Figure 2-3 and Figure 2-3, and use the other cursor to measure the peak by running it though the average final value of the waveform. Record the average value between the two cursors.

6. Record actual values.
7. Repeat steps 4 through 6 on the negative going waveform. Configure the oscilloscope using Table 2-3.
8. Confirm $+V_{OUT}$ and $-V_{OUT}$ fall within specification.

Note: $+V_{OUT}$ should be between 950 mV and 1050 mV. Although it is not specifically mentioned in specification 9.1.2.2, $-V_{OUT}$ should be between -950 mV and -1050 mV. Figure 2-2 and Figure 2-3 provide examples of data for the differential output voltage measurement.

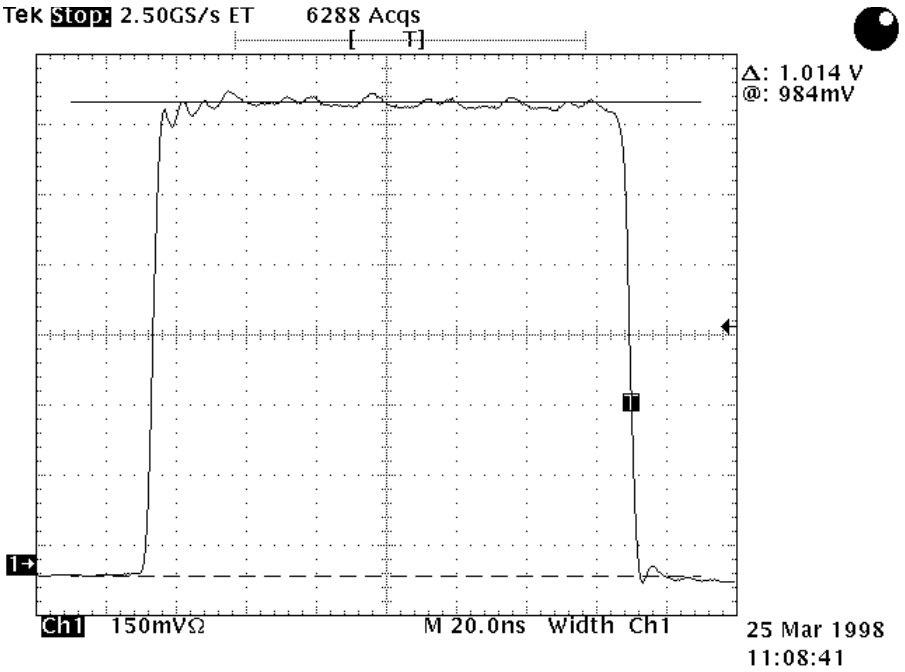

Figure 2-2. Positive Peak Differential Output Voltage (+Vpeak = 1.014 V)

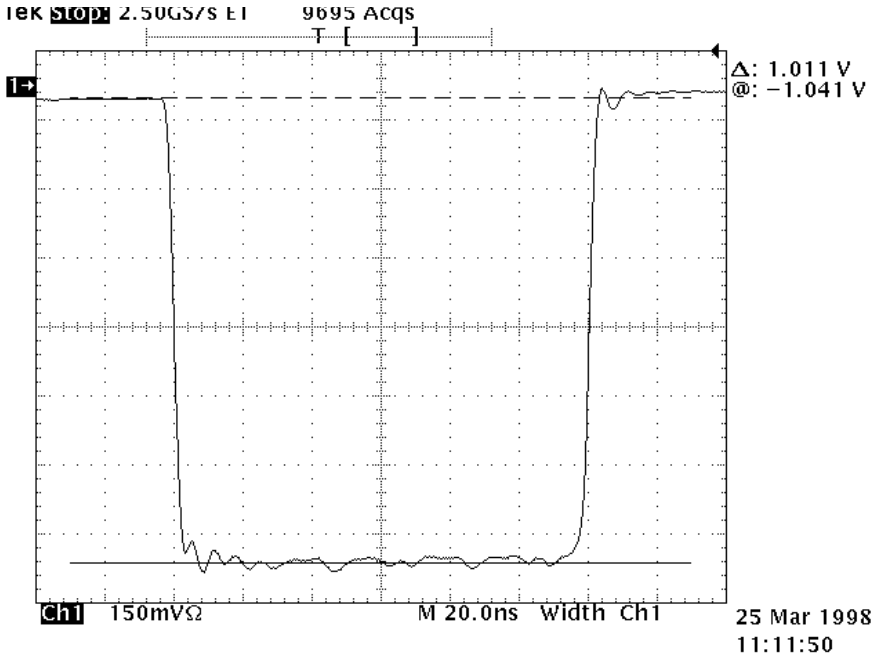

Figure 2-3. Negative Peak Differential Output Voltage (-Vpeak = 1.011 V)

3 100Base-TX Waveform Overshoot

ANSI SECTION 9.1.3

3.1 Test Purpose

To measure the overshoot of the differential waveform.

3.2 Specification

For the purposes of 9.1, overshoot is defined as the percentage excursion of the differential signal transition beyond its final adjusted value, VOUT, during the symbol interval following the signal transition. The adjusted value is obtained by performing a straight line best fit to an output waveform consisting of 14 bit times of no transition preceded by a transition from zero to either plus or minus VOUT as shown in Figure 3-1.

VOUT is defined to be the intersection of the straight line best fit for amplitude with the vertical line indicating the start of the transition from 0 V to VOUT.

The differential signal overshoot shall not exceed 5%. Any overshoot or undershoot transient shall have decayed to within 1% of the steady state voltage within [8.0] ns following the beginning of the differential signal transition.

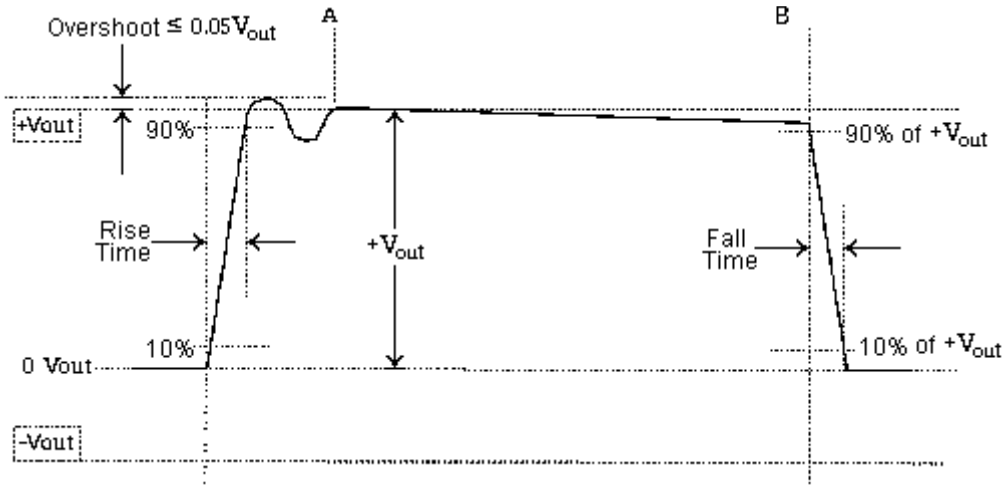

Figure 3-1. Waveform Overshoot at Active Output Interface

Based on ANSI X3.263-1995, p 29, Figure 12.

3.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

3.4 Test Fixtures

100 Ω UTP test load (Appendix D)

3.5 Test Procedure

1. Connect the test equipment and UUT as shown in Test Setup 1 in Appendix C.
2. Configure LANConf.exe as shown in Table 3-1.

Table 3-1. LANConf.exe Configuration for Waveform Overshoot

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	66 bytes
8	Transmit Threshold	66 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable •

• Denotes LANConf.exe default setting.

3. Begin transmitting.
4. Configure the oscilloscope according to Table 3-2.

Table 3-2. Setting for Positive Waveform Overshoot

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-150 mV to +1050 mV (1200 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	500 mV

Scope Parameter	Setting
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Table 3-3. Setting for Negative Waveform Overshoot

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-1125 mV to +75 mV (1200 mV over the full vertical scale)
Trigger Type	Negative pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	-500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 500 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 200 ns and the lower bound parameter to approximately 116 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

5. Select the horizontal cursors. Move one cursor to +VOUT and the other cursor to the maximum overshoot voltage.

Note: Overshoot is defined as the difference in voltage between the average peak voltage measured in Section 2, “100Base-TX Differential Output Voltage (UTP)” and the peak of the first ripple.

Note: If there is no overshoot visible in step 5, then overshoot settling time is not applicable. The tester should record “not applicable” for overshoot settling time, and testing for “100Base-TX Waveform Overshoot” is completed (make sure to check for both positive and negative waveform overshoot). However, if overshoot is present, the test should proceed to Step 6.

6. Calculate the overshoot by measuring the number of millivolts that the rising edge exceeds the positive or negative peak voltage (measured in Section 2, “100Base-TX Differential Output Voltage (UTP)”) and dividing the measured overshoot voltage by the corresponding peak voltage. Multiply the result by 100 to obtain the percentage.
7. Record the results.

8. Select the paired-dot cursors. Move one cursor to the zero voltage crossing and the other cursor to 8 ns beyond the first cursor position.
   The overshoot voltage shall have decayed to within 1% of the steady state voltage within 8 ns following the beginning of the differential signal transition.

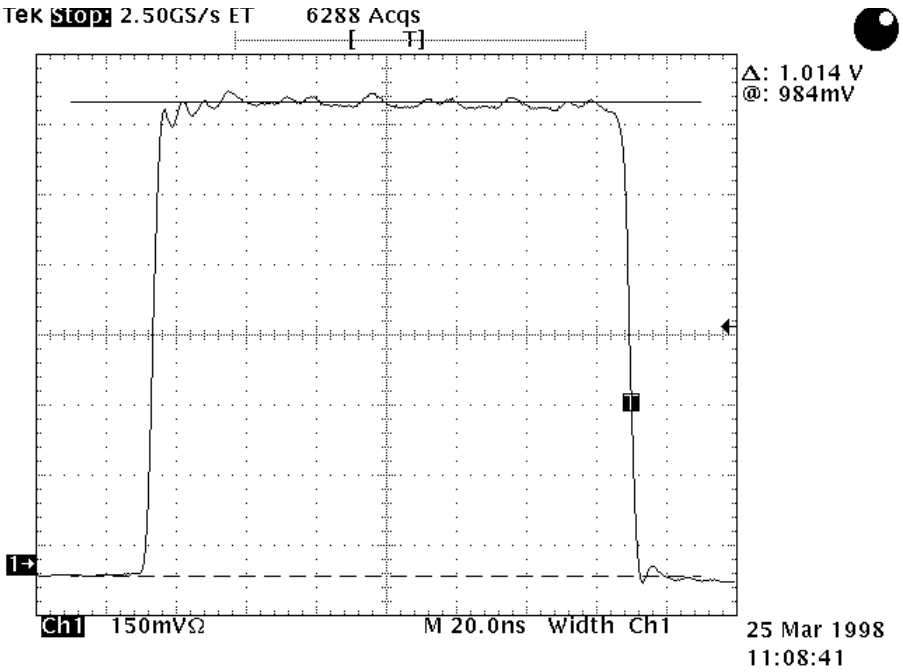

Figure 3-2. Positive Peak Waveform with No Overshoot on the Rising Edge

9. Repeat steps 4 through 8 using Table 3-3 to measure negative overshoot.

Example 1. Calculating Overshoot

If the negative peak voltage (the voltage delta between the MLT-3 mid-level and the negative pulse top) is -1000 mV and the overshoot voltage is 35 mV, then the percentage overshoot is:

$$\frac{35\text{mV}}{1000\text{mV}} \times 100 = 3.5\%$$

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4 100Base-TX Signal Amplitude Symmetry

ANSI SECTION 9.1.4

4.1 Test Purpose

To measure the voltage symmetry of the positive and negative waveforms.

4.2 Specification

The ratio of the +VOUT magnitude to -VOUT magnitude shall be between the limits:

$$0.98 \leq \frac{|V_{OUT}|}{|-V_{OUT}|} \leq 1.02.$$ [1]

4.3 Test Procedure

1. Perform test described in Section 2, “100Base-TX Differential Output Voltage (UTP)” if it has not already been done.
2. Calculate the ratio of +VOUT to -VOUT using the values from the results of Chapter 2, “100Base-TX Differential Output Voltage (UTP)”.
3. Record the results.

Example 1. Calculating the Ratio of +VOUT to -VOUT

From the plots in Section 2, “100Base-TX Differential Output Voltage (UTP)” (Figure 2-2 and Figure 2-3):

$$\frac{1.014V}{1.011V} = 1.003$$

$$0.98 \leq 1.003 \leq 1.02.$$

Note: $+V_{OUT}$ and $-V_{OUT}$ have the same units (V).

1. ANSI X3.263-1995, p 29.

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5 100Base-TX Transmitter Return Loss

ANSI Section 9.1.5

To measure the transmitter return loss.

5.1 Specification

The UTP... Active Output Interface shall be implemented such that the following return loss characteristics are satisfied for each of the specified line impedances.

- Greater than 16 dB from 2 MHz to 30 mHz
- Greater than (16 - 20log(f/30 MHz)) dB from 30 MHz to 60 MHz [where f = frequency]
- Greater than 10 dB from 60 MHz to 80 MHz

The impedance environment for the measurement of the UTP AOI return loss shall be 100 ± 15 Ω... The impedance [environment] shall be nominally resistive, with a magnitude of phase angle less than 3° over the specified measurement frequency range. [1]

5.2 Test Equipment

- Network analyzer (50 KHz to 500 MHz range)
- S-parameter test set (or transmission/reflection test set)
- Host computer running LANConf.exe

5.3 Test Fixtures

- 100Base-TX balun test fixture (Appendix D)
- BNC cable, with 50 Ω characteristic impedance
- Network analyzer calibration fixture (Appendix D)
- CAT5 twisted pair cable (under 6 inches in length)

5.4 Test Procedure

1. Turn on the network analyzer and let it warm up for five to ten minutes.
2. Reset network analyzer to factory default settings.
3. Select the S11 measurement parameter (if necessary).
4. Connect the test fixtures, UUT, and network analyzer as shown in Test Setup 2 in Appendix C. Make sure to connect the coaxial cable to the transmit balun.
5. Configure the network analyzer as shown in Table 5-1.

1. ANSI X3.263-1995, p 29-30.

Table 5-1. Network Analyzer Settings for Transmitter Return Loss

Analyzer Parameter	Setting
Start Frequency	1 MHz
Stop Frequency	101 MHz
Display Scale	5 dB/division
IF or Resolution Bandwidth	100 Hz
Triggering	Continuous
Display Points	401 (or as high as possible)

6. Disconnect the test fixture, but keep it close to the UUT.
7. Perform a 1-port, full calibration with an open, short, and 100 Ω load by connecting the calibration fixture to the RJ-45 connection in place of the UUT.

Note: It is important to try to keep the test setup as close as possible to its original position to achieve the best calibration.

8. Test the calibration by connecting the 50 Ω load and confirming the results are close to the theoretical value of 9.54 dB. Also verify that the open and short loads produce the expected results.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$ Balanced output impedance of the balun (for example, 100 Ω).

Z_{load} The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{|Z_{transmitter} + Z_{load}|}{|Z_{transmitter} - Z_{load}|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{|100\Omega + Z_{load}|}{|100\Omega - Z_{load}|}$$

For a 50 Ω load with the 100 Ω output of the balun, this becomes:

$$RL\_in\_dB = 20\log\frac{|100\Omega + 50\Omega|}{|100\Omega - 50\Omega|}$$

which simplifies to:

$$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54\ dB$$

9. Configure LANConf.exe as shown in Table 5-2.

Table 5-2. LANConf.exe Configuration for Transmitter Return Loss

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
12	Packet Sequence Numbers	Disable •

• Denotes LANConf.exe default setting.

The resulting display should be similar to Figure 5-1.

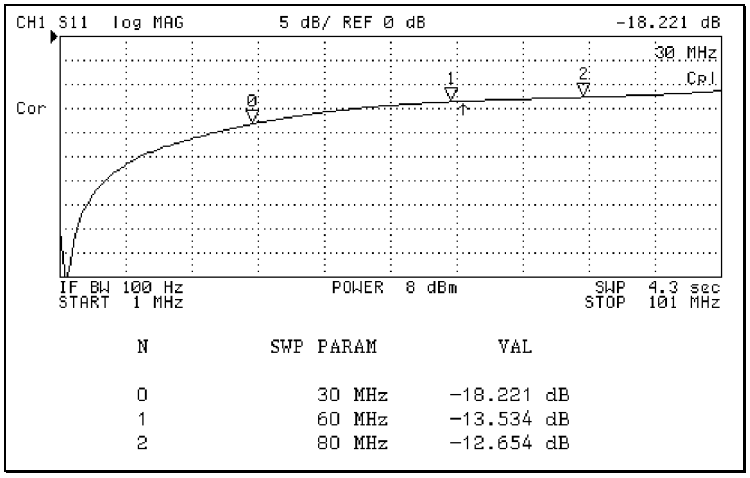

Figure 5-1. Transmitter Return Loss

10. Set the marker to the worst case return loss between 2 MHz and 30 MHz. Record the amplitude (dB of return loss).
11. Repeat step 10 from 30 MHz to 60 MHz and from 60 MHz to 80 MHz.

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6 100Base-TX Rise and Fall Times

ANSI SECTION 9.1.6

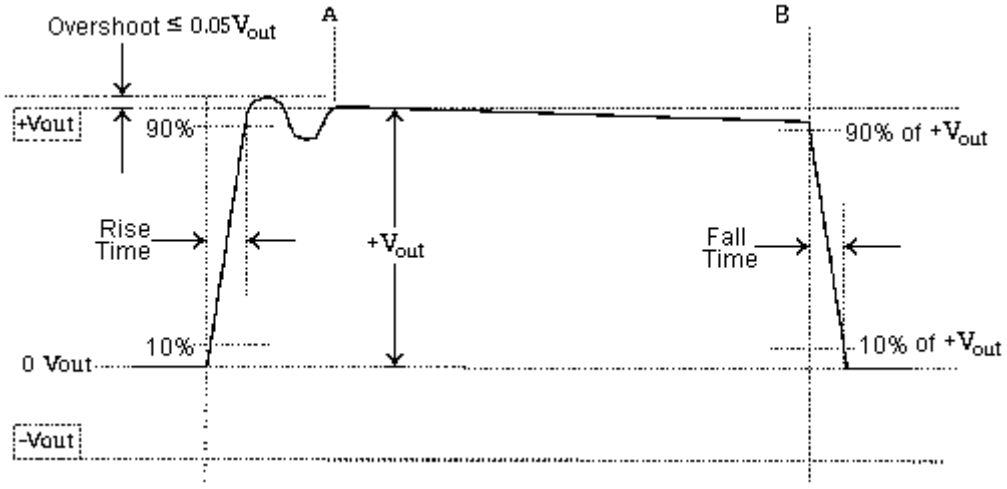
6.1 Test Purpose

To measure the rise and fall times of a non-scrambled bit pattern (both positive and negative waveforms need to be measured).

6.2 Specification

For the purposes of 9.1, the AOI signal rise is defined as a transition from the baseline voltage (nominally zero) to either +VOUT or -VOUT. Signal fall is conversely defined as a transition from the +VOUT or -VOUT to the baseline voltage.

The rise and fall times of the waveform shall be determined as the time difference between the 10% and the 90% voltage levels of the signal transition, where 100% is represented by VOUT of Figure 6-1. [1]



Based on ANSI X3.263-1995, p 29, figure 12

Figure 6-1. Waveform Overshoot at Active Output Interface

Measured rise and fall times shall be between the limits: 3.0 ns ≤ trise/fall ≤ 5.0 ns.The difference between the maximum and minimum of all measured rise and fall times shall be ≤ 0.5 ns."

6.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

1. ANSI X3.263-1995, p 30

ANSI X3.263-1995, p 30.

6.4 Test Fixtures

100 Ω UTP test load (Appendix D)

6.5 Test Procedure

1. Connect the test equipment and UUT as shown in Test Setup 1 in Appendix C.
2. Configure LANConf.exe as shown in Table 6-1.

Table 6-1. Setting for Positive Rise and Fall Times

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	66 bytes
8	Transmit Threshold	66 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable •

3. Begin transmitting.

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	66 bytes
8	Transmit Threshold	66 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable •

4. Configure the oscilloscope according to Table 6-2.

Table 6-2.

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	66 bytes
8	Transmit Threshold	66 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable •

Note: Denotes LANConf.exe default setting.

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 500 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 200 ns and the lower bound parameter to approximately 116 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

5. Locate the actual position of the peak voltage and the zero. Use the measurements from Section 2, "100Base-TX Differential Output Voltage (UTP)" plus the actual zero and peak voltage measurements to calculate the 10% and 90% voltage levels.
6. Zoom in on the positive waveform, expanding the rising edge of the wave to that it occupies as much of the screen as possible.
7. Select the split-dot (vertical pair) cursors. Move one cursor to 10% of $+V_{OUT}$ on the rising edge of the waveform and the other cursor to 90% of $+V_{OUT}$ on the rising edge as illustrated in Figure 6-2 and Figure 6-3.

Note: The rise time is the difference in time (Δt) between the two markers.

8. Repeat steps 6 and 7 for positive fall time.
9. Record the results. Confirm that the rise and fall times are between $3.0\ ns \leq t_{rise/fall} \leq 5.0\ ns$.

10. Repeat steps 5 through 9 for the negative-going waveform (Figure 6-4 and Figure 6-5).
11. Confirm that the difference between the maximum and minimum of all measured rise and fall times is less than or equal to 0.5 ns.

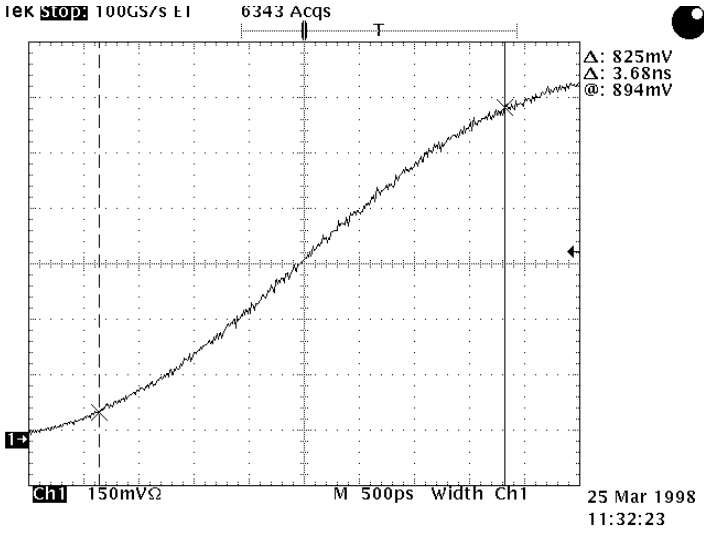


Figure 6-2. Positive Rise Time Measurement

Note: The rise time (Δt) in Figure 6-2 is measured to be 3.68 ns.

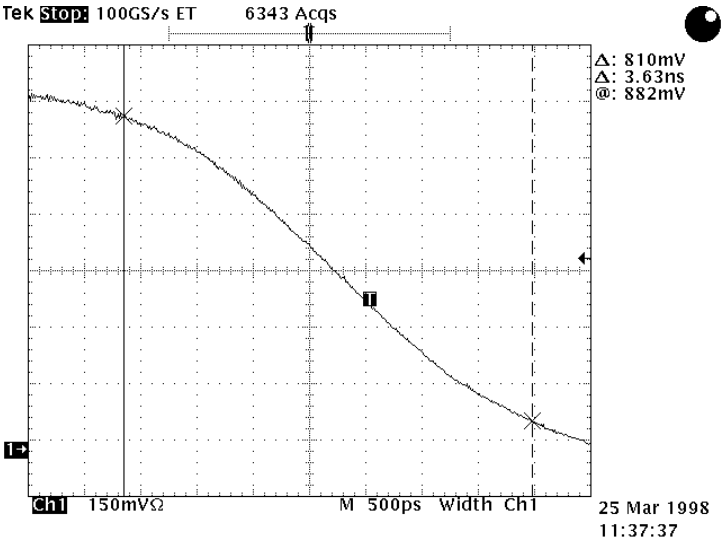


Figure 6-3. Positive Fall Time Measurement

Note: The fall time (Δt) in Figure 6-3 is measured to be 3.63 ns.

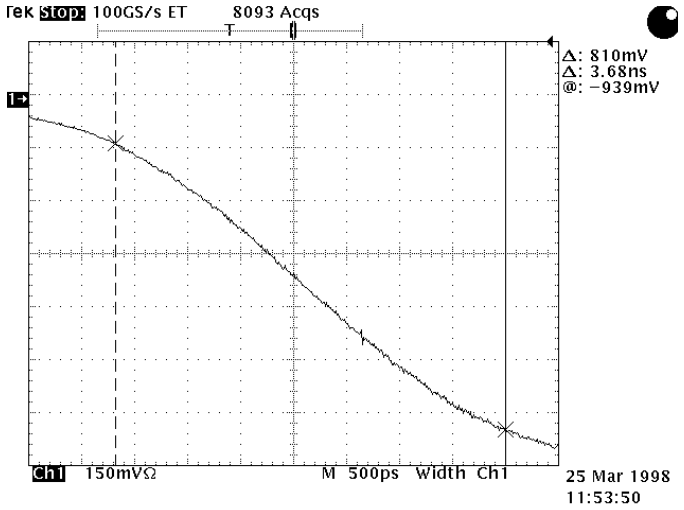


Figure 6-4. Negative Rise Time Measurement

Note: The rise time (Δt) in Figure 6-4 is measured to be 3.68 ns.

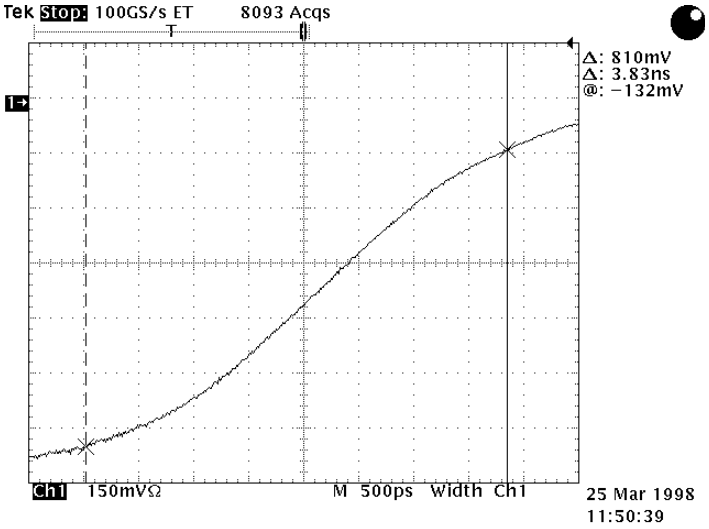


Figure 6-5. Negative Fall Time Measurement

Note: The fall time (Δt) in Figure 6-5 is measured to be 3.83 ns.

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7 100Base-TX Open Circuit Inductance (OCL)

ANSI Section 9.1.7

7.1 Test Purpose

To measure the inductance at the transmit pins of the UUT using the network analyzer.

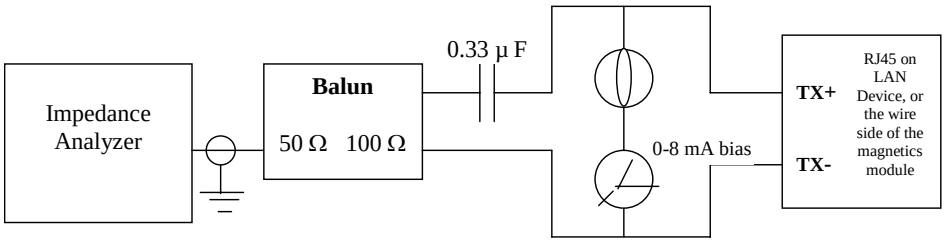
If the inductance level is greater than 350 mH, the transmitter should not have excessive baseline wander.

7.2 Specification

Baseline Wander tracking by the receiver is dependent on the worst case droop that can be produced by a transmitter. Droop is directly related to the Open Circuit Inductance (OCL) which varies with temperature, manufacturing tolerance, and bias current.

Worst case Baseline Wander Frames vary the transformer bias which causes the droop to change with data content. This variation must be accounted for by the receiver to track the Baseline Wander over long frames. Variation in inductance caused by bias of the transformer can be on the order of 2:1.

The minimum inductance measured at the transmit pins of the AOI shall be greater than or equal to 350 mH with any DC bias current between 0 mA and +8 mA injected as shown in Figure 7-1.[1]



Based on ANSI X3.263-1995, p 30, figure 13 Inductance Measurement Techniques.

Figure 7-1. Inductance Measurement with DC Bias

7.3 Test Equipment

- Network analyzer (50 KHz to 500 MHz range)
- Transmission/reflection test set
- Ammeter (must be able to measure granularity of 1 mA)

7.4 Test Fixtures

- Open circuit inductance test fixture (Appendix D)
- 6 V battery

1.ANSIX3.263-1995, p 30

- BNC cable, with 50 Ω characteristic impedance
- Network analyzer calibration fixture (Appendix D)
- CAT5 twisted pair cable (under 6 inches in length)

7.5 Test Procedure

Note: This test is optional and should be performed last. It is primarily a test of the magnetics, not the controller.

1. Turn on the network analyzer and let it warm up for five to ten minutes.
2. Lift the transmit pins on the PHY side of the magnetics module (TD+, TD-, and TDC).
3. Connect the test fixtures and UUT as shown in Test Setup 3 in Appendix C. Do not power-on the unit.
4. Set the test equipment to measure the impedance at 100 KHz.
5. Connect the magnetics module to the test fixture.
6. Adjust the DC bias to 8 mA.
7. Disconnect the UUT from the test fixture.
8. Calibrate the test equipment at the interface between the test fixture and the magnetics module.
9. Reconnect the magnetics module to the test fixture.
10. Record the OCL at 100 KHz with 8 mA DC bias current.
11. Confirm that OCL is greater than 350 mH.

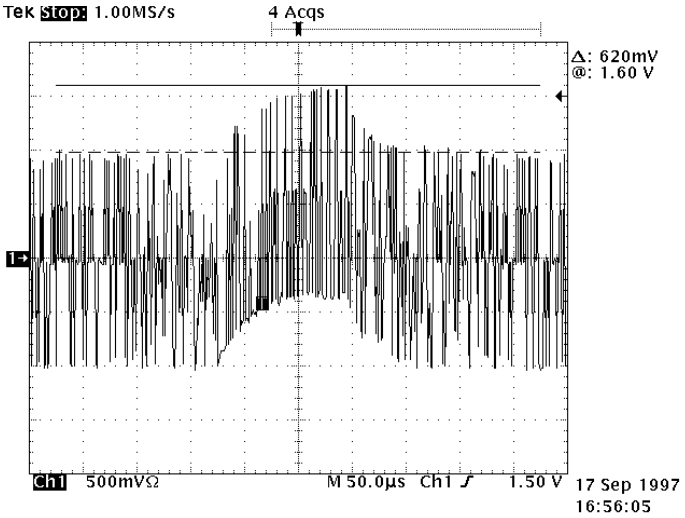


Figure 7-2. Example of Baseline Wander

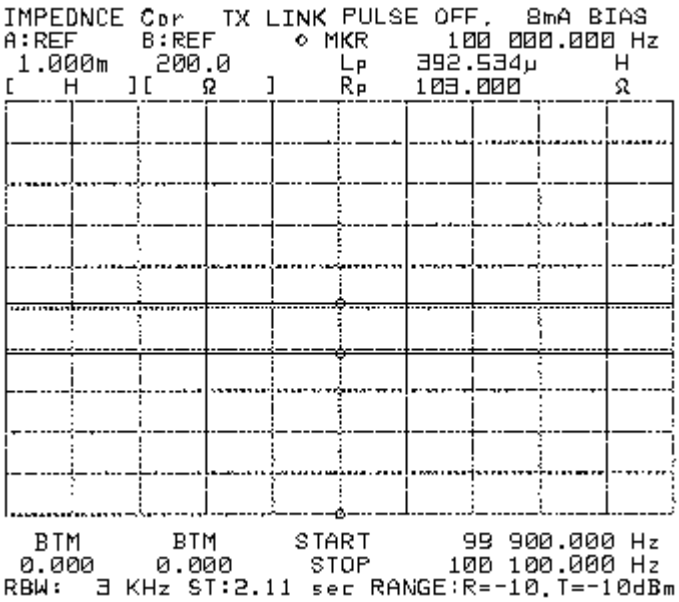


Figure 7-3. Open Circuit Inductance Data (from HP4195A)

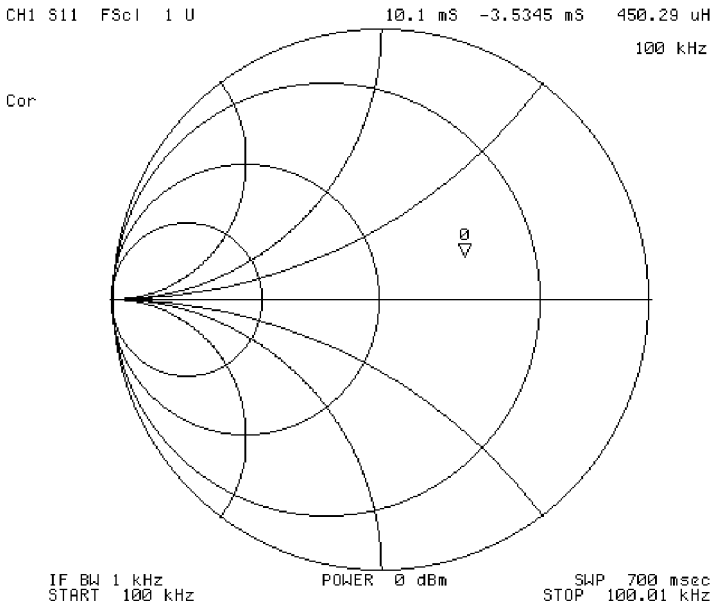


Figure 7-4. Open Circuit Inductance Data (from HP4396B)

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8 100Base-TX Duty Cycle Distortion (DCD)

ANSI SECTION 9.1.8

8.1 Test Purpose

To measure the duty cycle at the four MLT-3 transitions using a pattern in non-scrambled mode.

8.2 Specification

Duty cycle distortion shall be measured at the 50% voltage points on rise and fall transitions of the differential output waveform. The 50% times at the four successive MLT-3 transitions generated by a 01010101 NRZ [non-return to zero] bit sequence shall be used. The deviations of the 50% crossing times from a best fit to a time grid of 16 ns spacing shall not exceed ±0.25 ns as shown in Figure 8-1.[1]

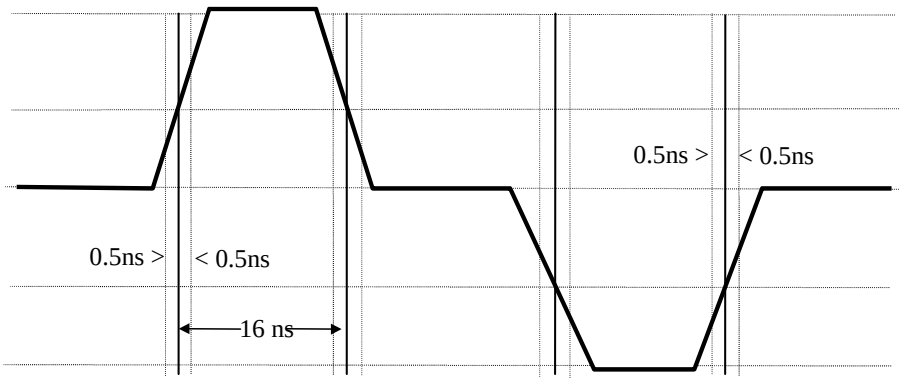

Figure 8-1. Active Output Interface Duty Cycle Distortion[2]

8.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

8.4 Test Fixtures

100 Ω UTP test load (Appendix D)

1.ANSI X3.263-1995, p 28
2.Based on ANSI X3.263-1995, p 30, figure 9-3.

8.5 Test Procedure

1. Connect the test equipment and UUT as shown in Test Setup 1 in Appendix C.
2. Configure LANConf.exe as shown in Table 8-1.

Table 8-1. LANConf.exe Configuration for Duty Cycle Distortion (DCD)

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Force
6	Duplex	Full Duplex (FD)
12	Packet Sequence Numbers	Disable •

Denotes LANConf.exe default setting.

3. Configure the oscilloscope according to the following table.

Table 8-2. Setting for Duty Cycle Distortion (DCD)

Scope Parameter	Setting
Horizontal Scale	~5 ns/division
Vertical Range	-1200 mV to +1200 mV (2400 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: ~14 ns lower bound, ~18 ns upper bound
Trigger Level	400 mV
Trigger Signal	16 ns positive pulse
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 400 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 30 ns and the lower bound parameter to approximately 2 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

4. Measure the relative peak voltage of the waveform.
5. Calculate the 50% values.

6. Zoom in on the waveform to get the best resolution.
7. Select the split-dot (paired) cursors. Move on cursor to +VOUT/2 on the rising edge of the waveform and move the other cursor to +VOUT/2 on the falling edge of the waveform.
8. Confirm that the deviations of the 50% crossing times do not exceed ±0.25 ns.
   In other words, the pulse should conform to the following: 15.50 ns ≤ Pulse Width ≤ 16.50 ns.
9. Record the results.
10. Repeat steps 4 through 9 for the mid-level negative waveform, as shown in Figures 8-3 through 8-5.

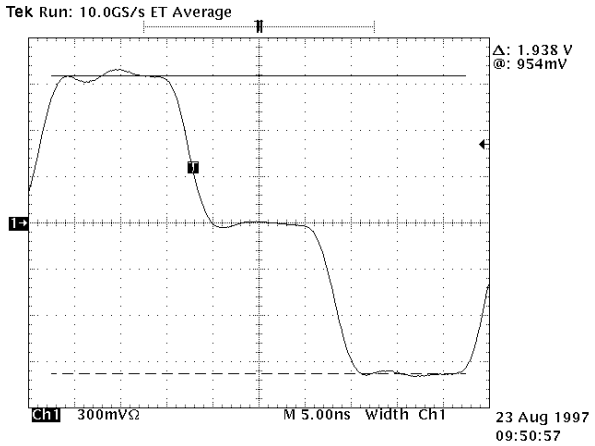

Figure 8-2. 16 ns Pulse Peaks Used to Calculate 50% Levels

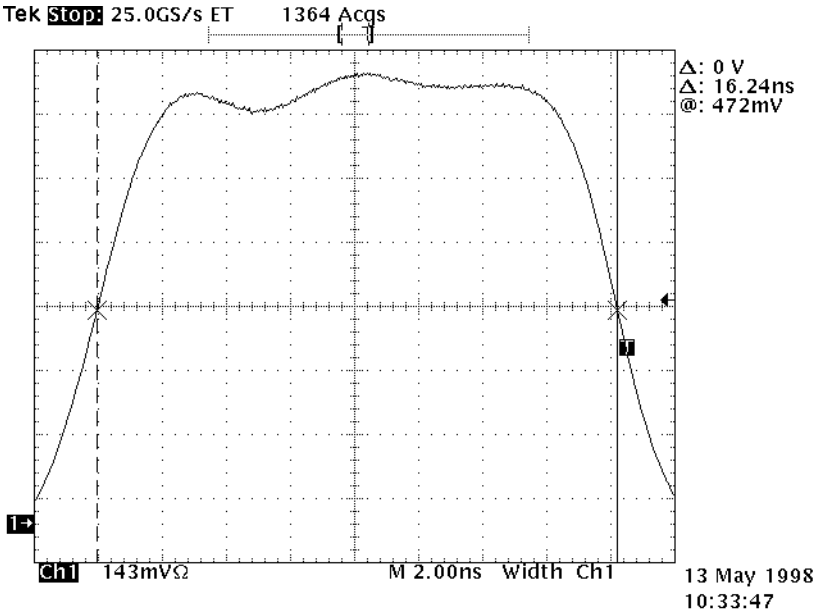

Figure 8-3. Positive Pulse Width at 50%

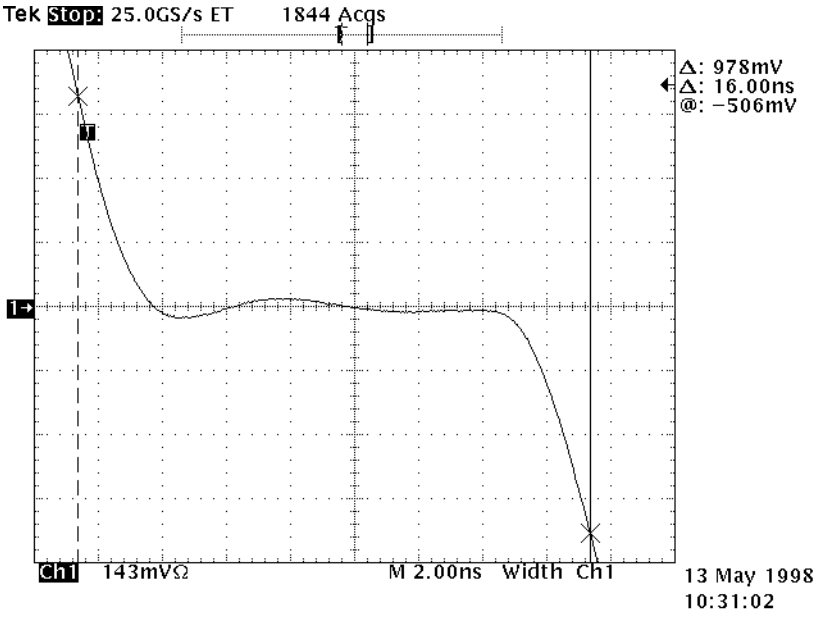

Figure 8-4. MLT-3 mid-level width at 50% levels

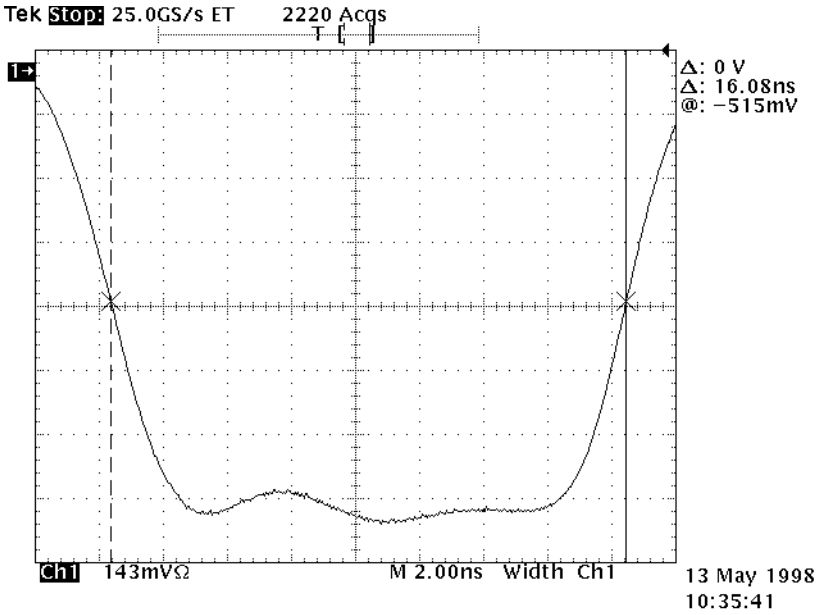

Figure 8-5. Negative pulse width at 50% amplitude level

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9 100Base-TX Transmit Jitter

ANSI SECTION 9.1.9

9.1 Test Purpose

To measure the jitter of a scrambled waveform output from the UUT.

9.2 Specification

"Peak to peak jitter shall be measured using the scrambled HALT line state. Total transmit jitter, including contributions from duty cycle distortion and Baseline Wander, shall not exceed 1.4 ns peak [to] peak.[1]

9.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

9.4 Test Fixtures

100 Ω UTP test load (Appendix D)

9.5 Test Procedure

1. Connect the test equipment and UUT as shown in Test Setup 1 in Appendix C.
2. Configure LANConf.exe as shown in Table 9-1.

Table 9-1. LANConf.exe Configuration for Transmit Jitter

	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Enabled • (Ena)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	64 bytes
8	Transmit Threshold	64 bytes
9	Transmit Pattern File	Random
12	Packet Sequence Numbers	Disable •

•Denotes LANConf.exe default setting.

1.ANSI X3.263-1995, p 31

3. Configure the oscilloscope according to the Table 9-2.

Table 9-2. Setting for Transmit Jitter

Scope Parameter	Setting
Horizontal Scale	~500 ps/division
Vertical Range	-800 mV to +800 mV (1600 mV over the full vertical scale)
Trigger Type	Positive edge triggering
Trigger Level	500 mV
Trigger Signal	Rising edge of all positive-going data signals
Display Type	Infinite persistence

4. Begin transmitting.
5. Scroll horizontally until an eye pattern is found similar to that shown in Figure 9-1.

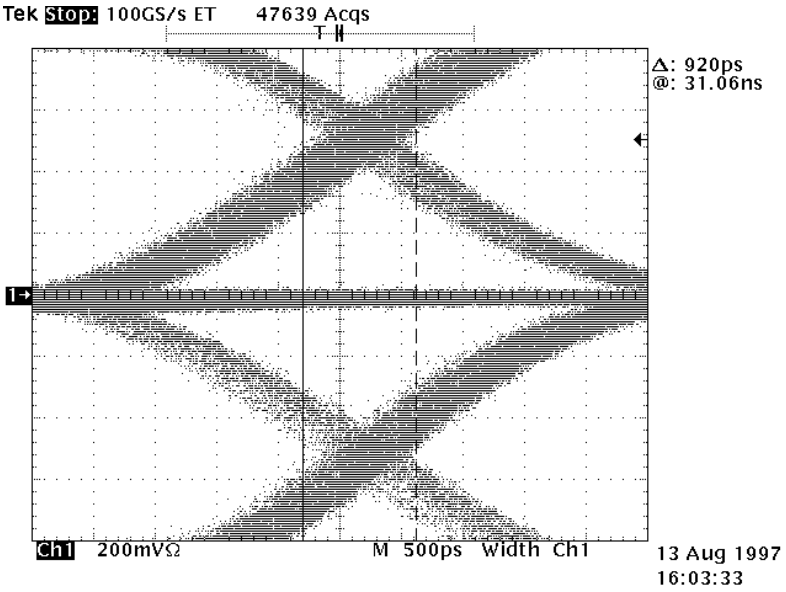

Figure 9-1. Transmit Jitter Data

6. Allow data to accumulate for one to ten minutes.
7. Use the scope's vertical bar cursors to measure the widest "X" as shown in Figure 9-1.
8. Record the results.
9. Confirm that the resulting jitter is less than 1.4 ns.

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10 100Base-TX Differential Input Signals (BER)

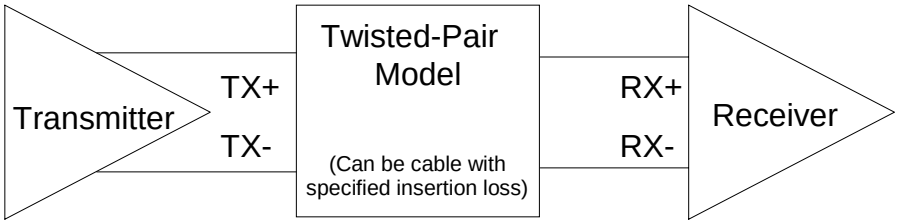
ANSI SECTION 9.2.1

10.1 Test Purpose

To measure the Bit Error Rate (BER) of the UUT over CAT5 cable with specified insertion loss.

10.2 Specification

The differential input signals, RD +/-, are defined at the output of the twisted pair model of annex A as shown in [Figure 10-1]. The differential transmitted signals on TD+/- meet the requirements of 9.1 (AOI). [1]



a. Based on ANSI X3.263, p 32, figure 15

Figure 10-1. Differential Input Signals

10.3 Test Equipment

- Transmit computer with either an Intel 82558 based Network Interface Card (NIC) or LAN On Motherboard (LOM) running LANConf.exe
- Host computer running LANConf.exe

10.4 Test Fixtures

Test cables 1 through 5 (or equivalent twisted pair models) (Appendix D)

10.5 Test Procedure

1. Power-up transmitting station and receiving station. Do not transmit any data until step 5 is completed.

Prepare Receiver

2. Connect transmit and receive units using a crossover cable or twisted pair model with specified insertion loss.
3. Reset the receiver's receive statistics counters (use the Dump Counters command under the CSMA/CD menu in LANConf.exe).
4. Configure LANConf.exe as shown in Table 10-1.

1.ANSI X3.263-1995, p 32

Table 10-1. Receiver LANConf.exe Configuration for Differential Input Signal

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enable
2	Force Good Link	Normal • (Norm)
3	Data Scrambling	Enable • (Ena)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Half Duplex • (HD)
10	Promiscuous Mode	Enable
11	Save Bad Frames	Enable •
12	Packet Sequence Numbers	Disable •
13	Broadcast	Enable •

Denotes LANConf.exe default setting.

5. Put the UUT into receive mode (through the LANConf.exe Transmit menu).

Prepare Transmitter

6. Reset the transmitter's transmit statistics counters (use the Dump Counters command under the CSMA/CD menu in LANConf.exe).
7. Configure LANConf.exe as shown in Table 10-2.

Table 10-2. Transmitter LANConf.exe Configuration for Differential Input Signal

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enable
2	Force Good Link	Normal • (Norm)
3	Data Scrambling	Enable • (Ena)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Half Duplex • (HD)
7	Transmit Packet Size	1024
8	Transmit Threshold	1024
9	Transmit Pattern File	Random
10	Promiscuous Mode	Disable •
11	Save Bad Frames	Enable •
12	Packet Sequence Numbers	Disable •
13	Broadcast	Enable •

Denotes LANConf.exe default setting.

Measure Bit Error Rate

8. Start transmitting frames.
9. Stop the transmitter after at least 2.5 million frames have been sent.
10. Stop the receiver.
11. Dump the transmit and receive statistics counters. Record the Good Transmit and Good Receive statistics.
12. Use the data from the counters to calculate the BER as shown in the following equation and example.

Note: The maximum BER is (1 x 10-8).

Calculating the Bit Error Rate (BER)

$$BER = \frac{GoodTransmit - GoodReceive}{TotalGoodTransmit} \times \frac{1}{\frac{bytes}{frame} \times 8\frac{bits}{byte}}$$

Example 10-1. Calculating Bit Error Rate

If 2,000,000 frames were transmitted, each frame is 1,024 bytes long, and 1,999,997 good frames were received, then:

$$BER = \frac{2,000,000 - (1,999,997)}{2,000,000} \times \frac{1}{1,024\frac{bytes}{frame} \times 8\frac{bits}{byte}}$$

$$BER = 1.83 \times 10^{-10}$$

Note: In this example, the BER is less than (1×10^{-8}), which is the maximum specification.

13. Repeat steps 2 through 12 for each cable length.

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11 100Base-TX Receiver Return Loss

ANSI SECTION 9.2.2

11.1 Test Purpose

To measure the receiver return loss.

11.2 Specification

The differential input impedance shall be such that the return loss is as shown below. The requirement is specified for any reflection due to differential signals incident upon RX +/- from a twisted pair having any impedance within the range specified in [ANSI X3.263 Section] 11.1.1. The return loss shall be maintained when the receiver circuit is powered.

- Greater than 16 dB from 2 MHz to 30 mHz
- Greater than (16 - 20log(f/30 MHz)) dB from 30 MHz to 60 MHz [where f = frequency
- Greater than 10 dB from 60 MHz to 80 MHz[1]

The impedance environment for the measurement of the UTP AII (Active Input Interface) return loss shall be 100 Ω ± 15 Ω. The impedance environment shall be nominally resistive with a magnitude of phase angle less than 3° over the specified measurement frequency range.

11.0 Test Equipment

- Network analyzer (50 KHz to 500 MHz range)
- S-parameter test set (or transmission/reflection test set)
- Host computer running LANConf.exe

11.1 Test Fixtures

- 100Base-TX balun test fixture (Appendix D)
- BNC cable, with 50 Ω characteristic impedance
- Network analyzer calibration fixture (Appendix D)
- CAT5 twisted pair cable (under 6 inches in length)

11.2 Test Procedure

1. Turn on the network analyzer and let it warm up for five to ten minutes.
2. Reset network analyzer to factory default settings.
3. Select the S11 measurement parameter if necessary.
4. Connect the test fixtures, UUT, and network analyzer as shown in Test Setup 2 in Appendix C. Make sure to connect the coaxial cable to the receive balun.

1.ANSI X3.263-1995, p 32.

5. Configure the network analyzer as shown in Table 11-1.

Table 11-1. Network Analyzer Settings for Receiver Return Loss

Analyzer Parameter	Setting
Start Frequency	1 MHz
Stop Frequency	101 MHz
Display Scale	5 dB/division
IF or Resolution Bandwidth	100 Hz
Triggering	Continuous
Display Points	401 (or as high as possible)

6. Disconnect the test fixture, but keep it close to the UUT.
7. Perform a 1-port, full calibration with an open, short, and 100 Ω load by connecting the calibration fixture to the RJ-45 connection in place of the UUT.

Note: It is important to try to keep the test setup as close as possible to its original position to achieve the best calibration.

8. Test the calibration by connecting the 50 Ω load and confirming the results are close to the theoretical value of 9.54 dB. Also verify that the open and short loads produce the expected results.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$ Balanced output impedance of the balun (for example, 100 Ω).

Z_{load} The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{|Z_{transmitter} + Z_{load}|}{|Z_{transmitter} - Z_{load}|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{|100\Omega + Z_{load}|}{|100\Omega - Z_{load}|}$$

For a 50 Ω load with the 100 Ω output of the balun, this becomes:

$$RL\_in\_dB = 20\log\frac{|100\Omega + 50\Omega|}{|100\Omega - 50\Omega|}$$

which simplifies to:

$$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54\ dB$$

9. Configure LANConf.exe as shown in Table 11-2.

Table 11-2. LANConf Configuration for Receiver Return Loss

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
12	Packet Sequence Numbers	Disable •

Denotes LANConf default setting.

10. Reconnect the test fixture to the UUT.

The resulting network analyzer display should be similar to Figure 11-1.

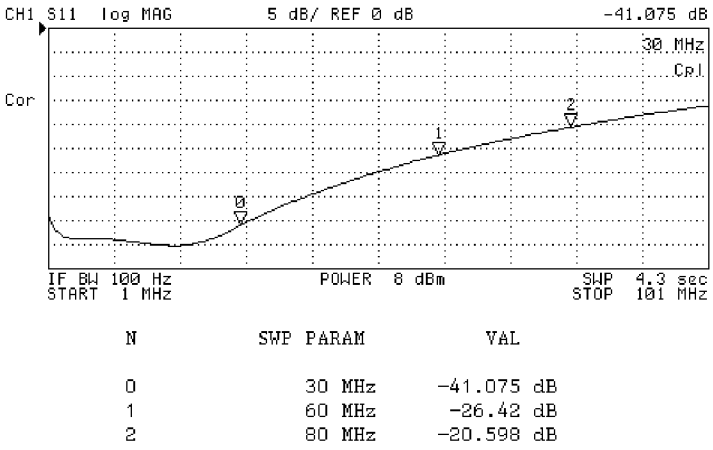

Figure 11-1. Receiver Return Loss Data

11. Set the marker to the worst case return loss between 2 MHz and 30 MHz. Record the amplitude (dB of return loss).

12. Repeat step 11 from 30 MHz to 60 MHz and from 60 MHz to 80 MHz.

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12 100Base-TX Receiver Common Mode Rejection

ANSI SECTION 9.2.3

12.1 Test Purpose

To test the receiver unit's tolerance to common mode voltage (Ecm).

12.2 Specification

Receiver shall deliver the proper value for PM-UNITDATA.indication[1], at the specified Bit Error Rate, for any signal meeting the requirements of [ANSI X3.263-1995 Section] 10.1. The receiver shall deliver the correct value for Ecm applied as shown in [Figure 12-1]. Ecm shall be a [1.0] V peak-to-peak sine wave from 0 MHz to 125 MHz.

The impedance of the [test] equipment shall not disrupt the impedance of the channel.

Note: Implementers are encouraged to test to the applicable country EMC standards.

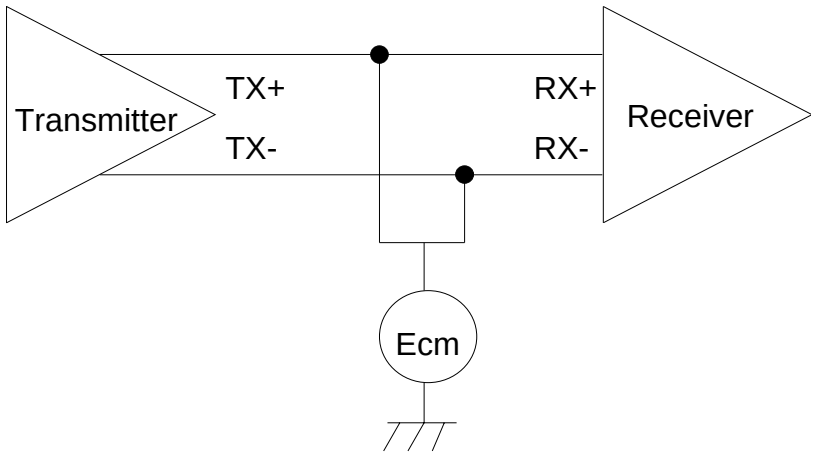

Figure 12-1. Common Mode Rejection[2]

12.3 Test Equipment

- Network analyzer (50 KHz to 500 MHz range) or swept signal generator (capable of generating a 1 V peak-to-peak sine wave, 100 KHz to 125 MHz)
- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Transmit computer with either an Intel 82558 based Network Interface Card (NIC) or LAN On Motherboard (LOM) running LANConf.exe

1.Defined in ANSI X3.263-1995, section 6.1.2, p 13.
2.Based on ANSI X3.263-1995, p 33, figure 16

- Host computer running LANConf.exe

[1] Defined in ANSI X3.263-1995, Section 6.1.2, p 13

12.4 Test Fixtures

- BNC cable with 50 Ω characteristic impedance
- BNC to hook clip
- Receiver common mode rejection test fixture (Appendix D)
- Test cables 1 through 5 (Appendix D)

12.5 Test Procedure

Setting Up the Network Analyzer (or Swept Signal Generator)

1. Turn on the network analyzer and let it warm up for 10 to 15 minutes.
2. Connect the equipment, cables, and test fixtures as illustrated in Test Setup 4 in Appendix C.

Note: It is possible to use the signal generator which is built into the vector network analyzer. If possible, do not use a transmission/reflection test set.

3. Power-up the receive adapter (in other words, the UUT) and force it to 100Base-TX mode.
4. Put the network analyzer into S11 mode.
5. Turn the transmit adapter off.

Note: Turning off the transmit adapter reduces noise on the cable, allowing the injected noise to be measured more accurately.

6. Configure the network analyzer as shown in Table 12-1.

Table 12-1 Network Analyzer Settings for Receiver Common Mode Rejection

Analyzer Parameter	Setting
Start Frequency	100 KHz [1]
Stop Frequency	1.6 MHz
Display Scale	5 dB/division
IF or Resolution Bandwidth	100 Hz
Triggering	Continuous
Display Points	401 (or as high as possible)
Sweep Time	5 s
Output Voltage	950 mV to 1050 mV across the entire frequency range

1. The start and stop should be adjusted so that the amplitude is between 950 mV and 1050 mV across the entire frequency range. All steps must be repeated for each range from 100 KHz to 125 MHz.

7. Configure the oscilloscope as shown in Table 12-2.

Table 12-2 Oscilloscope Settings for Receiver Common Mode Rejection

Scope Parameter	Setting
Horizontal Scale	Set to achieve the best view of the frequency range output of the network analyzer (or signal generator)
Vertical Range	-525 mV to +525 mV (1050 mV over the full vertical scale)
Horizontal Cursors	+475 mV and -475 mV (950 mV delta between the two cursors)
Trigger Type	Positive edge
Trigger Level	300 mV
Trigger Signal	Sinusoidal input from network analyzer (or signal generator)
Display Type	Average

8. Adjust the network analyzer's internal transmit attenuator to fall within the range specified above while using the oscilloscope and differential probes to measure the amplitude of the signal at the input to the receiver. If the voltage swing is too great, than the frequency span will need to be decreased (lower the stop frequency).

Caution: Always verify the output of the network analyzer (or signal generator) with an oscilloscope with high impedance/low capacitance probes. Signal generator output amplitude and frequency seldom match the front panel settings. Signal generator amplitude variations can be caused by different output loads (input impedance of UUT) and by variations, aging components, etc. The frequency of the signal generator may not match front panel values.

12.6 Setting Up the Transmitting and Receiving Stations

9. Power-up the transmitting and receiving stations. Do not transmit any data until Step 15 is complete.

Prepare Receiver

10. Reset the receiver's transmit statistics counters (use the Dump Counters command under the CSMA/CD menu in LANConf.exe).
11. Configure LANConf.exe as shown in Table 12-3 for the receiver.

Table 12-3 Receiver LANConf.exe Configuration for Receiver Common

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enable
2	Force Good Link	Normal • (Norm)
3	Data Scrambling	Enable • (Ena)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Half Duplex • (HD)
10	Promiscuous Mode	Enable
11	Save Bad Frames	Enable •
12	Packet Sequence Numbers	Disable •
13	Broadcast	Enable •

12. Put the UUT into receive mode (through the LANConf.exe Transmit menu).

Prepare Transmitter

13. Reset the transmitter's transmit statistics counters (use the Dump Counters command under the CSMA/CD menu in LANConf.exe).
14. Configure LANConf.exe as shown in Table 12-4 for the transmitter.

Table 12-4 Transmitter LANConf.exe Configuration for Receiver Common Mode Rejection

Setting Number	LANConf.exe Setting	Status
1	Force 100	Enable
2	Force Good Link	Normal • (Norm)
3	Data Scrambling	Enable • (Ena)
4	4b/5b Encoding	Normal • (Norm)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Half Duplex • (HD)
7	Transmit Packet Size	1024
8	Transmit Threshold	1024
9	Transmit Pattern File	Random
10	Promiscuous Mode	Disable •
11	Save Bad Frames	Enable •
12	Packet Sequence Numbers	Disable •
13	Broadcast	Enable •

15. Start transmitting frames.
16. Stop the transmitter after at least 2.5 million frames have been sent.
17. Stop the receiver.

18. Dump the transmit and receive statistics counters. Record the transmit and receive statistics.
19. Use the data from the counters to calculate the BER.

Note: The maximum BER is (1 x 10-8).

Calculating the Bit Error Rate (BER)

$$BER = \frac{GoodTransmit - GoodReceive}{TotalGoodTransmit} \times \frac{1}{\frac{bytes}{frame} \times 8\frac{bits}{byte}}$$

An example calculation is shown in .

20. Repeat steps 5 through 19, changing the start and stop frequencies each time until the whole 100 KHz to 125 MHz frequency range has been covered.

Note: Each portion of the swept frequency band should be as wide as possible without violating the requirements described in Step 8.

21. Repeat the entire procedure for test cables 1 through 5.

Chapter 10, “100Base-TX Differential Input Signals (BER)”,

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13 10Base-T Peak Differential Output Voltage on TD Circuit

IEEE STANDARD 14.3.1.2.1

13.1 Test Purpose

To verify the TD circuit peak differential output voltage

13.2 Specification

The peak differential output voltage on the TD circuit when terminated with a 100-ohm resistive load shall be between 2.2 V-pk and 2.8 V-pk for all data sequences.

13.3 Test Equipment

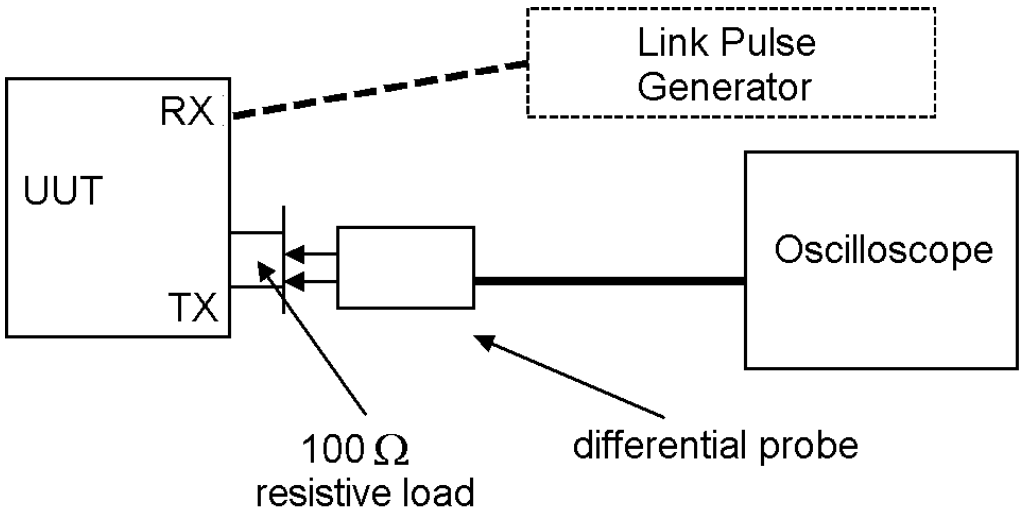
- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater Bandwidth)
- Host computer running LANConf.exe
- Link pulse generator (if link integrity cannot be disabled)

13.4 Test Fixtures

100 Ω resistive load (Appendix D)

13.5 Test Procedure

1. Connect the test equipment and UUT as shown below.



2. Configure LANConf.exe as shown in the table below.

Table 13-1 LANConf.exe Configuration for Peak Differential Output Voltage on TD Circuit

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	64 bytes
8	Transmit Threshold	64 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable •

3. Configure the oscilloscope according to the table below.

Table 13-2 Scope Configuration for Peak Differential Output Voltage on TD Circuit

Horizontal Scale	10 to 50 ms/division
Vertical Scale	-3.1 V to +3.1 V (at 10 vertical divisions, use 620 mV/division; at 8 divisions, use 775 mV/division)
Trigger Type	Pulse width: ~148 ns (lower bound); ~364 ns (upper bound)
Trigger Level	Typically 0.5 V to 1.7 V.

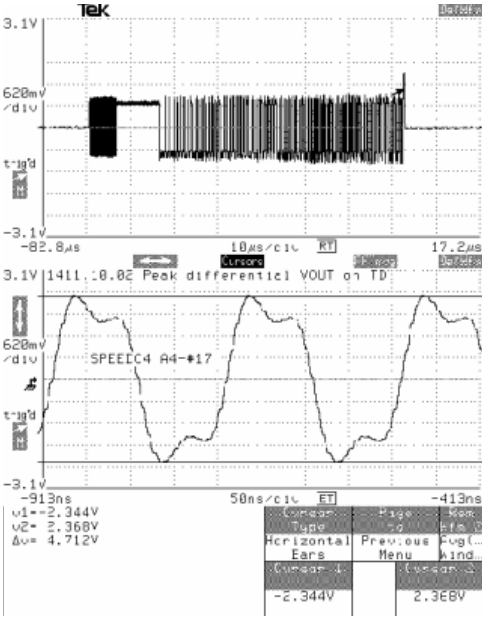
Pulse Width Triggering

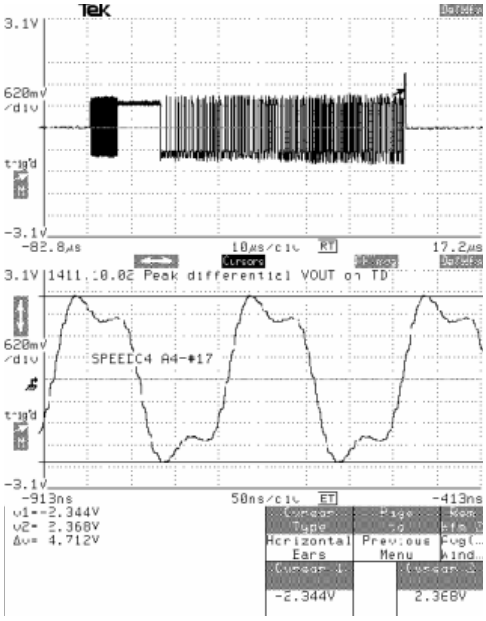
Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level as specificed in the above table.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

4. Ensure link integrity is disabled or use a link pulse generator.
5. Locate the 5 MHz and 10 MHz signals after a stable trigger is obtained and measure positive and negative peak voltages.

6. Locate regions of three periods for each signal to ensure the peak voltage is not affected by transitioning from a 5 MHz signal to a 10 MHz signal or from a 10 MHz signal to a 5 MHz signal. The following figures provide references.





7. Record the values.
8. Confirm the values fall within the specification.

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14 10Base-T Harmonic Content

IEEE STANDARD 14.3.1.2.1

14.1 Test Purpose

To verify the harmonic content at the transmitter output.

14.2 Specification

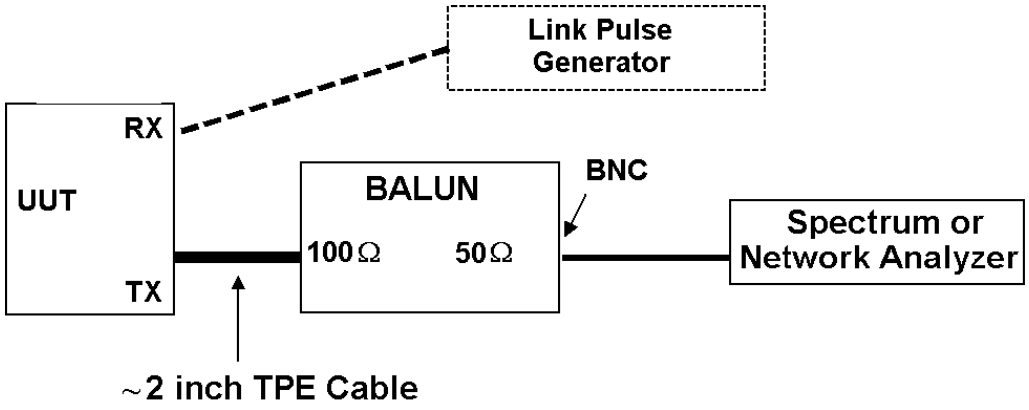
When the UUT is driven by an all ones Manchester signal, each harmonic measured at the output of the transmitter shall be at least 27 dB below the fundamental frequency.

14.3 Test Equipment

- Spectrum Analyzer
- CAT 5 twisted pair cable (under 2 inches in length)
- BNC cable, with 50-ohm characteristic impedance
- Link pulse generator (if link integrity cannot be disabled)

14.4 Test Fixtures

Balun Test Fixture with 200 MHz or greater bandwidth (Appendix D).



14.5 Test Procedure

1. Insert CAT 5 cable into transmitter side of Balun fixture and connect Balun to Spectrum Analyzer (or Network Analyzer) through a BNC cable as shown above.
2. Configure LANConf as shown in the table below.

Table 14-1 LANConf.exe Configuration for Harmonic Content

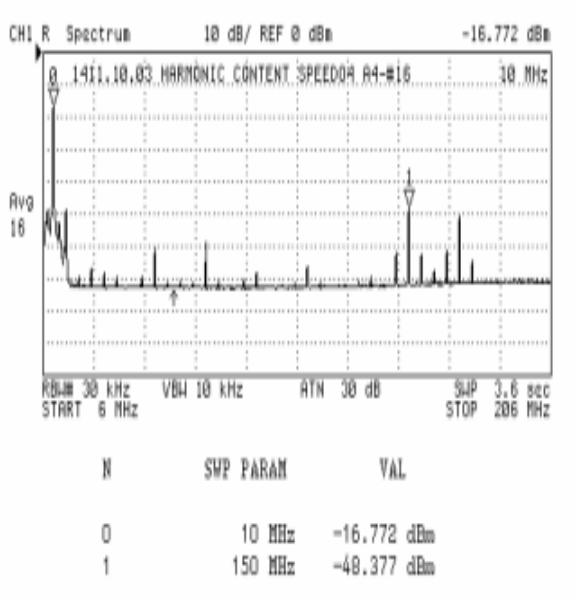
Setting Number	LANConf.exe Setting	Status
1	Force 10	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal • (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	1500 bytes
8	Transmit Threshold	1500 bytes
9	Transmit Pattern File	Manchester encodeded 1s
12	Packet Sequence Numbers	Disable •

3. Adjust the spectrum analyzer as indicated below.

Table 14-2 Analyzer Configuration for Harmonic Content

Start Frequency	6 MHz
Stop Frequency	206 MHz (a pre-scan to 500 MHz is okay)
Resolution BW or IF BW	Lowest practical BW supported by equipment in the range of 10 KHz and 200 KHz.
Number of Points (Resolution)	Maximum for instrument (≥ 401)
Acquire	Average (if necessary)
Vertical Division	10 dB/division
Mode	Spectrum Analyzer

4. Transmit 1500 byte length frames of Manchester-encoded 1's at the fastest rate possible.
5. Ensure link integrity is disabled or use a link pulse generator.
6. Place a marker on 10 MHz (fundamental frequency) and the highest amplitude harmonic (must be a multiple of 10 MHz) between 6 MHz and 206 MHz. The figure below provides a reference.



Note: For a better display, The end frequency can be reduced to be closer to the frequency of the highest amplitude harmonic.

Note: The signal may need to be attenuated if it is out of range on the spectrum analyzer.

7. Record dBm at 10 MHz and dBm at highest amplitude harmonic. The difference between the two markers must be greater than 27 dBm to ensure compliance with IEEE standards and specifications.
8. Confirm the values fall within the specifications.

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15 10Base-T TD Circuit Impedance (Transmitter Return Loss)

IEEE STANDARD 14.3.1.2.2

15.1 Test Purpose

To measure the transmitter return loss.

15.2 Specification

The return loss shall be Š 15dB from 5 MHz to 10 MHz

15.2.1 Test Equipment

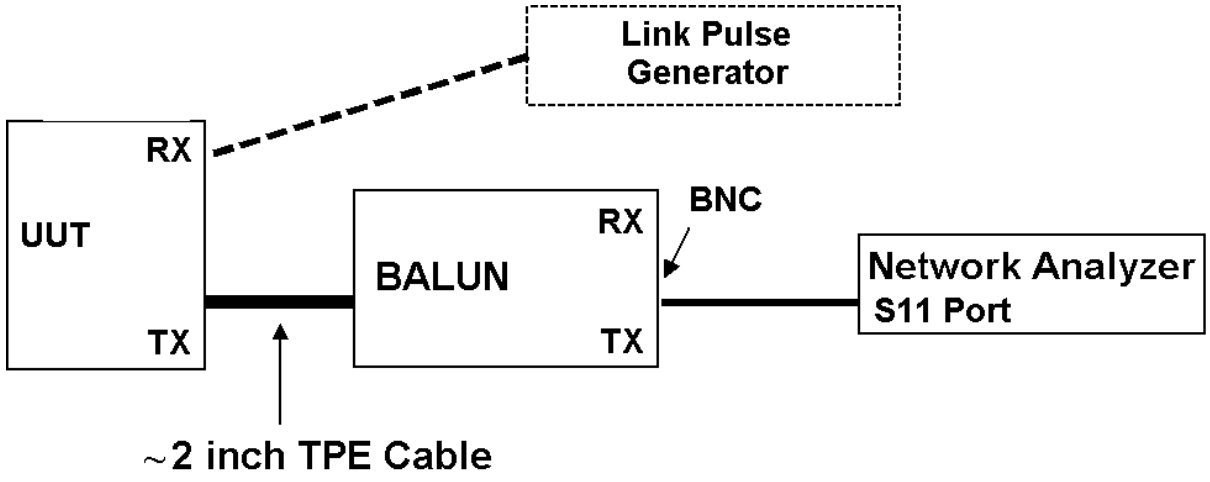
- Network Analyzer
- CAT 5 twisted pair cable (under 2 inches in length)
- BNC cable, with 50-ohm characteristic impedance
- Link pulse generator (if link integrity cannot be disabled)

15.3 Test Fixtures

- Balun Test Fixture with 200 MHz or greater bandwidth (Appendix D).
- Load Fixture for Network Analyzer calibration (Appendix D).Test Procedure

1. Insert CAT 5 cable from the UUT into transmitter side of Balun fixture and connect Balun to Network Analyzer with BNC cable as shown below.

Figure 15-1

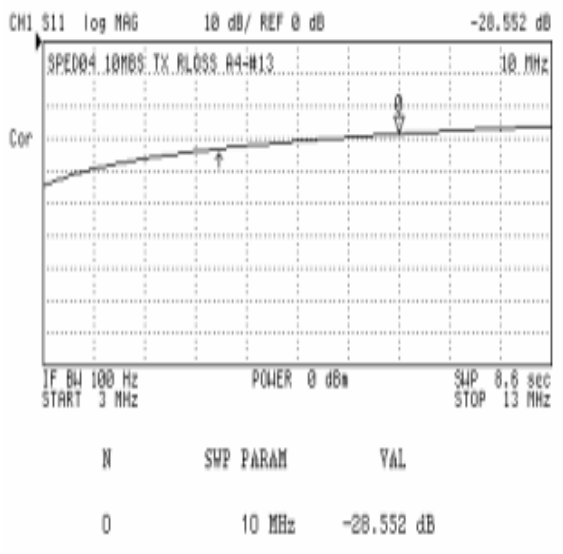


2. Adjust the spectrum analyzer to the following settings.

Table 15-1 Analyzer Configuration for TD Circuit Impedance

Start Frequency	3 MHz
Stop Frequency	13 MHz
IF BW or Resolution BW	Lowest practical bandwidth supported by equipment in the range of 100 KHz and 200 KHz.
Number of Points (Resolution)	Maximum for instrument (≥ 401)
Acquire	Average (if necessary)
Vertical Division	10 dB/division
Mode	Network Analyzer

3. Ensure the UUT is in 10 Mbps mode.
4. Ensure link integrity is disabled or use a link pulse generator.
5. Perform a calibration on the S11, S-parameter, port and turn correction on.
6. Use the 50 Ω load to verify the calibration. The return loss should be between 9.5 dB and 9.6 dB.
7. Set the marker to the worst-case return loss between 5 MHz and 10 MHz inclusive. (The figure below provides a reference.)



8. Record the amplitude (dB) of the return loss.
9. Confirm the value falls within the specification.

16 10Base-T TD Circuit Common-Mode Output Voltage

IEEE STANDARD 14.3.1.2.5

16.1 Test Purpose

To measure and record the common-mode output voltage of the transmitter.

16.2 Specification

Common-mode voltage shall be less than 50 mV peak.

16.3 Test Equipment

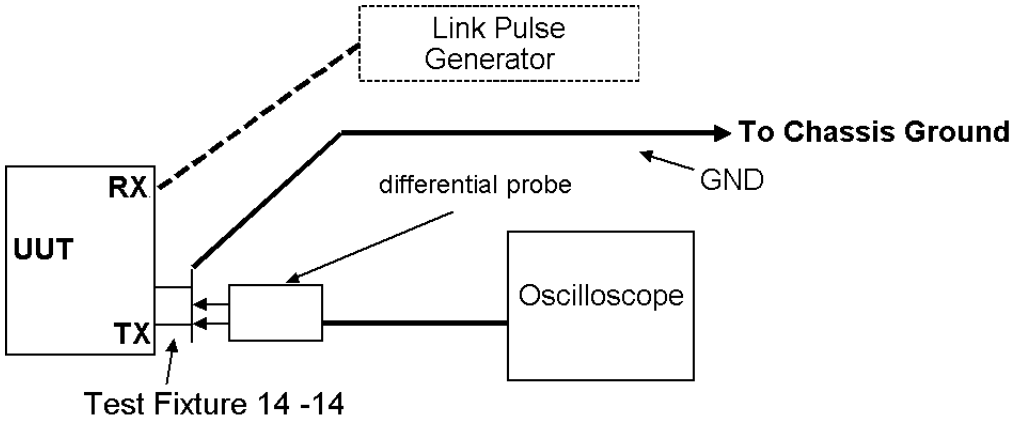
- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater bandwidth)
- Computer running LANConf.exe
- Link pulse generator (if link integrity cannot be disabled)

16.4 Test Fixtures

Test Fixture 14-14 (Appendix D)

16.5 Test Procedure

1. Insert test fixture into the UUT and attach differential probe and BNC cable to common-mode terminals on the fixture as shown below.



2. Configure LANConf.exe as shown in table below.

Table 16-1 LANConf.exe Configuration for TD Circuit

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	64 bytes
8	Transmit Threshold	64 bytes
9	Transmit Pattern File	User Specified, 000880.pat
12	Packet Sequence Numbers	Disable

3. Transmit 64-byte (512 bits) length frames of random data.

Note: Transmitting at the fastest rate allows better display and triggering.

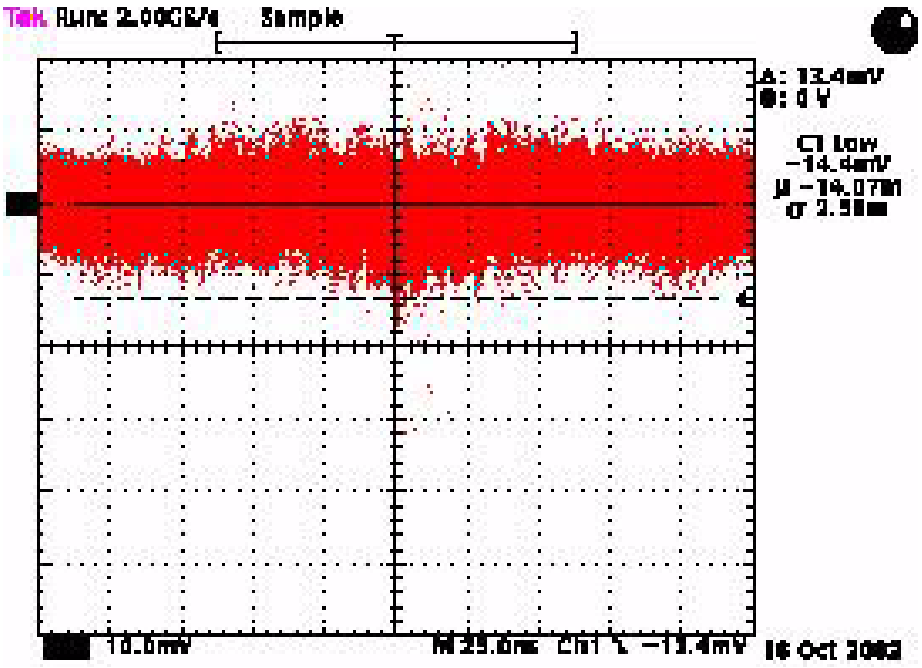
4. Ensure link integrity is disabled or use a link pulse generator.
5. Set scope settings for positive common-mode measurement as shown in table below.

For positive common-mode measurement:

Table 16-2 Scope Configuration for TD Circuit

Horizontal Scale	25 ns/division
Vertical Scale	-80 mV to +80 mV (at 8 divisions, this equals 20 mV/ division)
Trigger Type	Positive edge
Trigger Level	Typically 0 V to +50 mV
Display Persistence	Infinite persistence

6. Adjust trigger level until just triggering on signal. Place cursor on maximum or peak voltage. (The figure below provides a reference for the positive peak.)



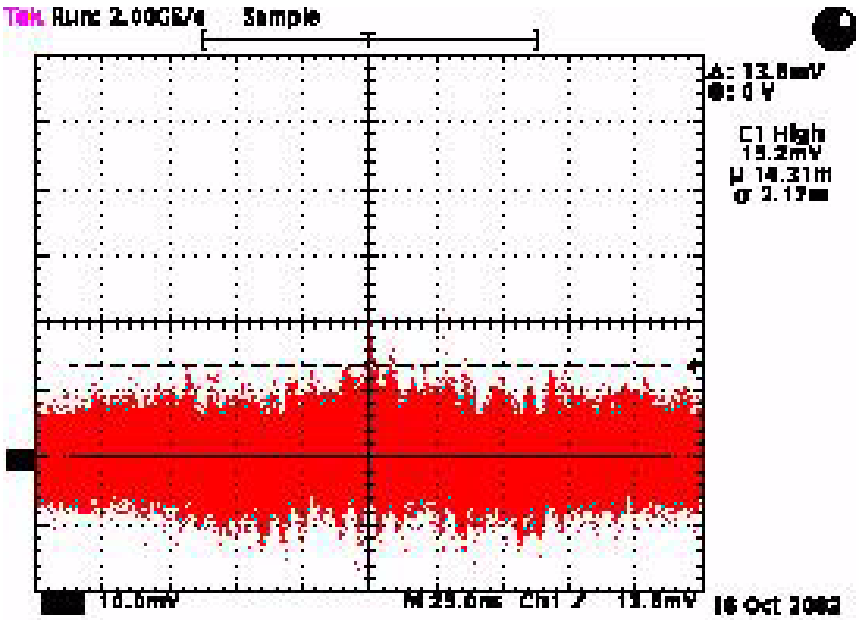
7. Record max peak positive amplitude value.
8. Set scope settings for negative common-mode measurement as shown in table below.

For negative common-mode measurement:

Table 16-3 Scope Configuration for TD Circuit

Horizontal Scale	10 ns/division
Vertical Scale	-80 mV to +80 mV (at 8 divisions, this equals 20 mV/ division)
Trigger Type	Negative edge
Trigger Signal	Differential signal
Trigger Level	Typically 0 V to -50 mV
Display Persistence	Infinite persistence

9. Adjust trigger level until just triggering on signal. Place cursor on maximum or peak voltage. (The figure below provides a negative peak reference.)



10. Record maximum or peak amplitude value(s).
11. Ensure the values fall within the specifications.

17 10Base-T Transmitter Output Timing Jitter with Cable Model

IEEE STANDARD 14.3.1.2.3

17.1 Test Purpose

To verify the jitter added by the UUT.

17.2 Specification

The jitter added to the signal on the DO circuit as it propagates through the UUT and twisted pair model shall be no more than 12.0 ns.

17.2.1 Test Equipment

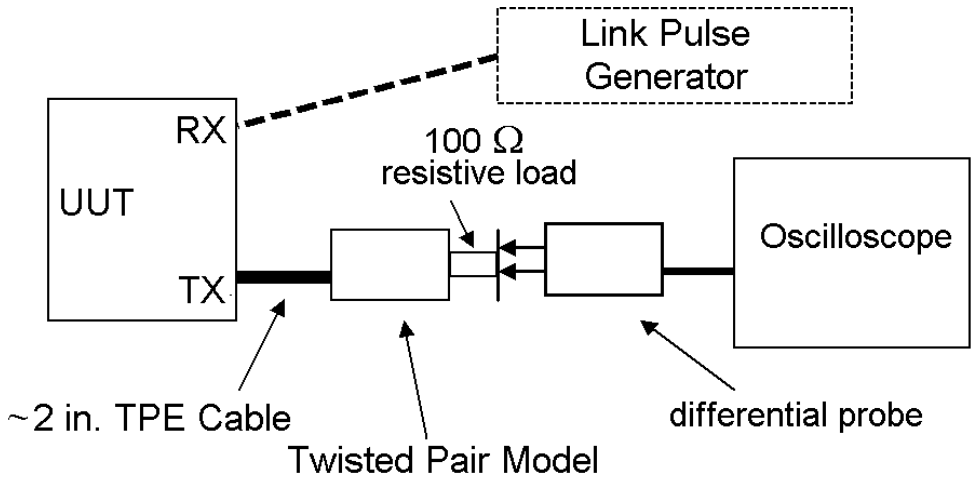
- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater bandwidth)
- CAT 5 twisted pair cable (under 2 inches in length)
- Link pulse generator (if link integrity cannot be disabled)

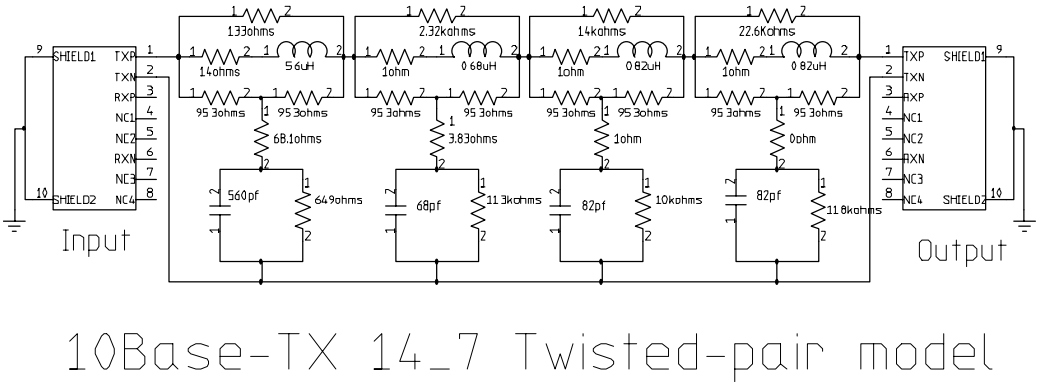
17.3 Test Fixtures

- 100-ohm resistive load (Appendix D)
- Twisted pair model

17.4 Test Procedure

1. Insert CAT 5 cable, connected to twisted pair model, into UUT and attach differential probe to the test load as shown below.





2. Configure LANConf.exe as shown in Appendix 17-1below.

Table 17-1 LANConf.exe Configuration for Transmit Output Jitter

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	1500 bytes
8	Transmit Threshold	1500 bytes
9	Transmit Pattern File	Random
12	Packet Sequence Numbers	Disable

3. Configure the oscilloscope according to table below.

Table 17-2 Scope Configuration for Peak Differential Output on TD Circuit

Horizontal Scale	10 ms/division
Vertical Scale	-600 mV to +600 mV (at 10 vertical divisions, this equals 120 mV/division; at 8 divisions, 150 mV/division)
Trigger Type	Pulse width: ~220 ns (lower bound); ~320 ns (upper bound) Tight trigger (±10 ns of actual pulse width) is best.
Trigger Level	Typically 0.5 V to 1.7 V
Display Persistence	Infinite persistence

Pulse Width Triggering

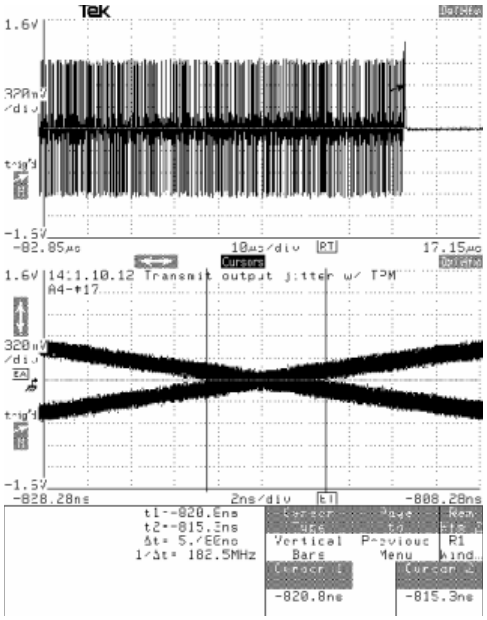
Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level as specificed in the above table.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

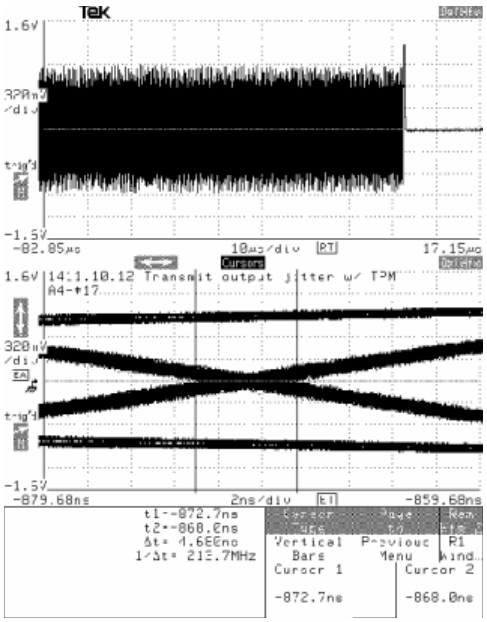
4. Transmit 1500-byte length frames of random data.

Note: Transmitting at the fastest rate allows better display and triggering.

5. Ensure link integrity is disabled or use a link pulse generator.
6. Shift waveform to the right and find zero crossing at 8.0 BT ±7ns (approximately 800 ns). The graphic below provides a reference.



7. Set vertical cursors to record the maximum closing of the eye.
8. Shift waveform to the right and find zero crossing at 8.5 BT ±7ns (approximately 850 ns). The graphic below provides a reference.
9. Set vertical cursors to record maximum closing of the eye.



10. Ensure the values fall within the specifications.

18 10Base-T Transmitter Output Timing Jitter without Cable Model

IEEE STANDARD 14.3.1.2.3

18.1 Test Purpose

To verify the jitter added by the UUT when directly driving a 100 Ω resistive load.

18.2 Specification

The jitter added to the signal on the DO circuit as it propagates through the UUT, driving a 100-ohm resistive load, shall be no more than 11.0 ns.

18.3 Test Equipment

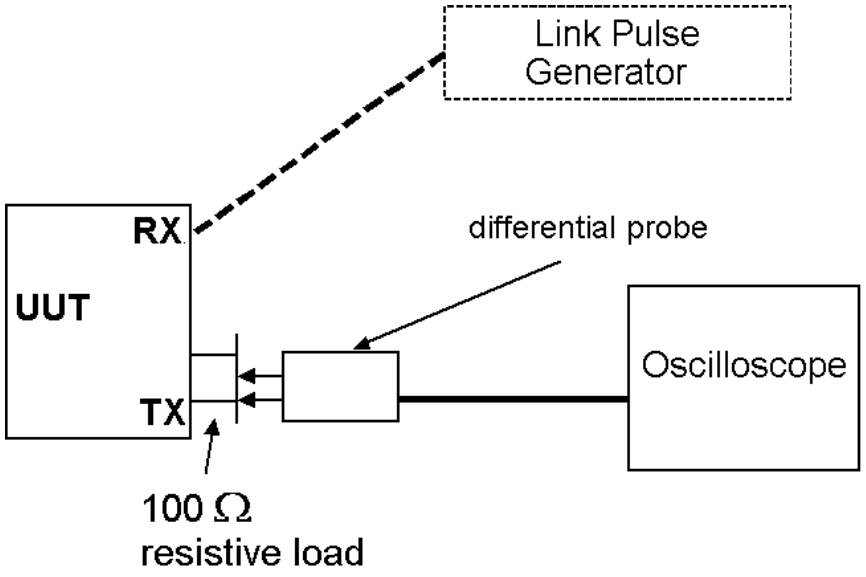
- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater bandwidth)
- CAT 5 twisted pair cable (under 2 inches in length)
- Link pulse generator (if link integrity cannot be disabled)

18.4 Test Fixtures

- 100-ohm resistive load (Appendix D)

18.5 Test Procedure

1. Insert CAT 5 cable into UUT and attach differential probe to the test load as shown below.



2. Configure LANConf.exe as shown in the table below.

Table 18-1 LANConf.exe Configuration for Transmitter Output Timing Jitter without Cable Model

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enabled
2	Force Good Link	Force
3	Data Scrambling	Disabled (Dis)
4	4b/5b Encoding	Bypass (Byp)
5	3/4 Encoding	Normal (Norm)
6	Duplex	Full Duplex (FD)
7	Transmit Packet Size	1500 bytes
8	Transmit Threshold	1500 bytes
9	Transmit Pattern File	Random
12	Packet Sequence Numbers	Disable

3. Configure the oscilloscope according to the table below.

Table 18-2 Scope Configuration for Peak Differential Output Voltage on TD Circuit

Horizontal Scale	10 ns/division
Vertical Scale	-1.6 V to +1.6 V (at 10 vertical divisions, use 320 mV/division; at 8 divisions, 400 mV/division)
Trigger Type	Pulse width: ~220 ns (lower bound); ~320 ns (upper bound) Tight trigger (±10 ns of actual pulse width) is best.
Trigger Level	Typically 0.5 V to 1.7 V
Display Persistence	Infinite persistence

Pulse Width Triggering

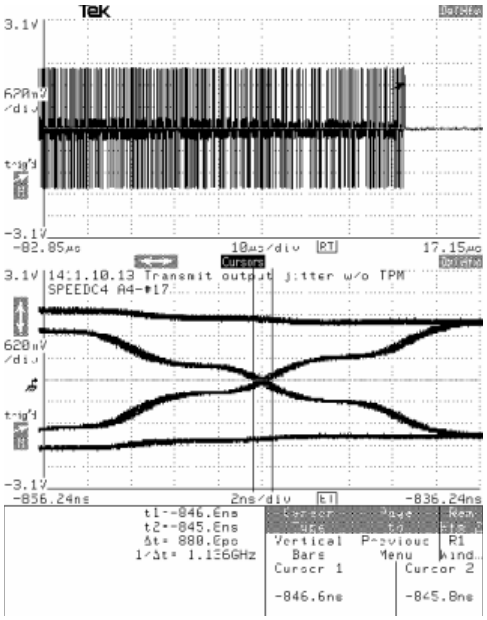
Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level as specificed in the above table.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

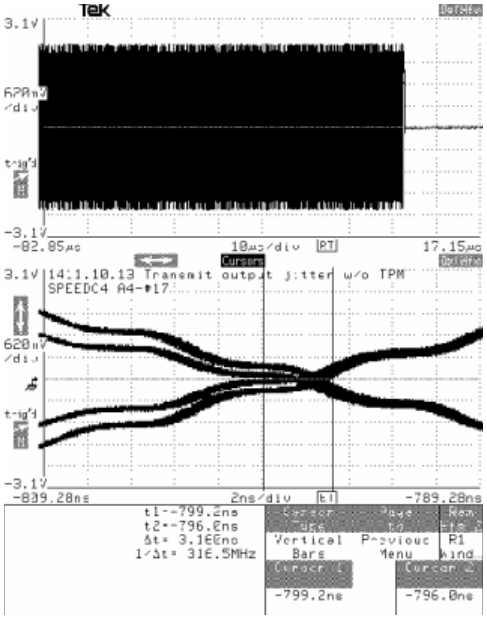
4. Transmit 1500-byte length frames of random data.

Note: Transmitting at the fastest rate allows better display and triggering.

5. Ensure link integrity is disabled or use a link pulse generator.
6. Shift waveform to the right and find zero crossing at 8.0 BT ±7 ns (approximately 800 ns). (The graphic below provides a reference.)



7. Set vertical cursors to record the maximum closing of the eye.
8. Shift the waveform to the right and find zero crossing at 8.5 BT ±7 ns (approximately 850 ns).



9. Set vertical cursors to record the maximum closing of the eye.
10. Ensure the values fall within the specifications.

19 10Base-T RD Receiver Circuit Signal Acceptance Test (BER)

19.1 Test Purpose

To measure the Bit Error Rate (BER) of the UUT over CAT3 cable with specified insertion loss.

19.2 Specification

The differential input signals, RD+/-, are defined at the output of the twisted pair model of annex A as shown in Figure 19-1. The differential transmitted signals on TD+/- meet the requirements of 9.1 (AOI).[1]

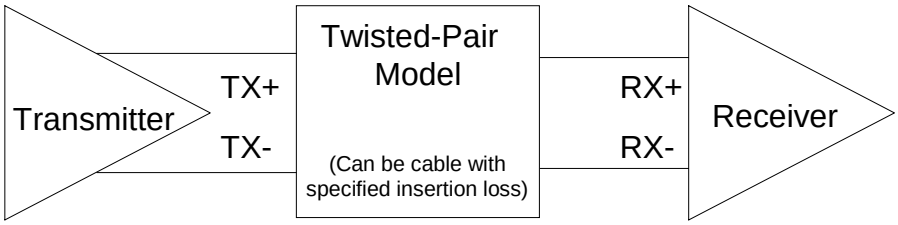


Table 19-1. Differential Input Signals[2]

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enable
2	Force Good Link	Normal (Norm)
3	Data Scrambling	Enable (Ena)
4	4b/5b Encoding	Normal (Norm)
5	3/4 Encoding	Normal (Norm)
6	Duplex	Half Duplex (HD)
10	Promiscuous Mode	Enable
11	Save Bad Frames	Enable
12	Packet Sequence Numbers	Disable
13	Broadcast	Enable

19.3 Test Equipment

- Transmit computer with either an Intel 82558 based Network Interface Card (NIC) or LAN On Motherboard (LOM) running LANConf.exe

1.ANSI X3.263-1995, p 32
2.Based on ANSI X3.263, p 32, figure 15.

- Host computer running LANConf.exe

19.4 Test Fixtures

CAT 3 cable cut to 10 dB attenuation

19.5 Test Procedure

1. Turn on transmitting station and receiving station. Do not transmit any data until Step 5 is completed.

Prepare Receiver

2. Connect transmit and receive units using a crossover cable or twisted pair model with specified insertion loss.
3. Reset the receiver's receive statistics counters (use the Dump Counters command under the CSMA/CD menu in LANConf.exe).
4. Configure LANConf.exe as shown in Table 19-1.

Table 19-2. Receiver LANConf.exe Configuration for Differential Input Signal

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enable
2	Force Good Link	Normal (Norm)
3	Data Scrambling	Enable (Ena)
4	4b/5b Encoding	Normal (Norm)
5	3/4 Encoding	Normal (Norm)
6	Duplex	Half Duplex (HD)
7	Transmit Packet Size	1024
8	Transmit Threshold	1024
9	Transmit Pattern File	Random
10	Promiscuous Mode	Disable
11	Save Bad Frames	Enable
12	Packet Sequence Numbers	Disable
13	Broadcast	Enable

5. Put the UUT into receive mode (through the LANConf.exe Transmit menu).

Prepare Transmitter

6. Reset the transmitter's transmit statistics counters (use the Dump Counters command under the CSMA/CD menu in LANConf.exe).
7. Configure LANConf.exe as shown in Table 19-2.

Table 19-3. Transmitter LANConf.exe Configuration for Differential Input Signal

Setting Number	LANConf.exe Setting	Status
1	Force 10	Enable
2	Force Good Link	Normal (Norm)
3	Data Scrambling	Enable (Ena)
4	4b/5b Encoding	Normal (Norm)
5	3/4 Encoding	Normal (Norm)
6	Duplex	Half Duplex (HD)
7	Transmit Packet Size	1024
8	Transmit Threshold	1024
9	Transmit Pattern File	Random
10	Promiscuous Mode	Disable
11	Save Bad Frames	Enable
12	Packet Sequence Numbers	Disable
13	Broadcast	Enable

Calculating the Bit Error Rate (BER)

$$BER = \frac{GoodTransmit - GoodReceive}{TotalGoodTransmit} \times \frac{1}{\frac{bytes}{frame} \times 8\frac{bits}{byte}}$$

Example 19 1. Calculating Bit Error Rate

If 2,000,000 frames were transmitted, each frame is 1,024 bytes long, and 1,999,997 good frames were received, then:

$$BER = \frac{2,000,000 - (1,999,997)}{2,000,000} \times \frac{1}{1,024\frac{bytes}{frame} \times 8\frac{bits}{byte}}$$

$$BER = 1.83 \times 10^{-10}$$

Note: In this example, the BER is less than (1 x 10^{-8}), which is the maximum specification.

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20 10Base-T RD Circuit Differential Input Impedance (Receiver Return Loss)

IEEE STANDARD 14.2.1.4

20.1 Test Purpose

To verify the differential input impedance.

20.2 Specification

The return loss shall be greater than or equal to 15 dB from 5 MHz to 10 MHz.

20.3 Test Equipment

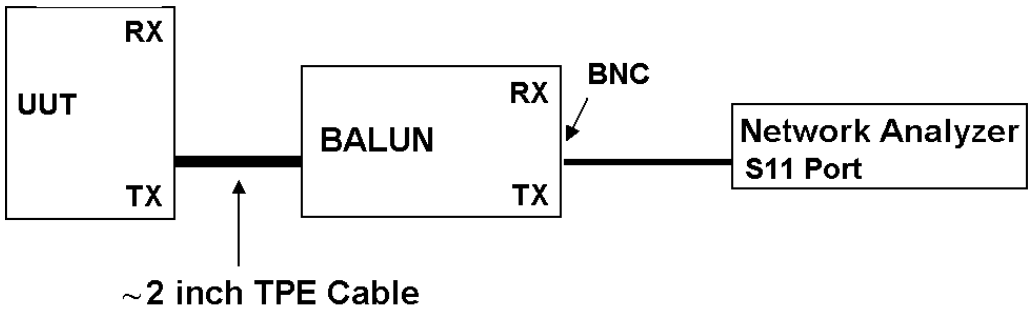
- Network Analyzer
- CAT 5 twisted pair cable (under 2 inches in length)
- BNC cable, with 50-ohm characteristic impedance

20.4 Test Fixtures

- Balun Test Fixture with 200 MHz or greater bandwidth (Appendix D)
- Load Fixture for Network Analyzer calibration (Appendix D)

20.5 Test Procedure

1. Insert CAT 5 cable from UUT into transmitter side of Balun fixture and connect Balun to Network Analyzer with BNC cable as shown below.

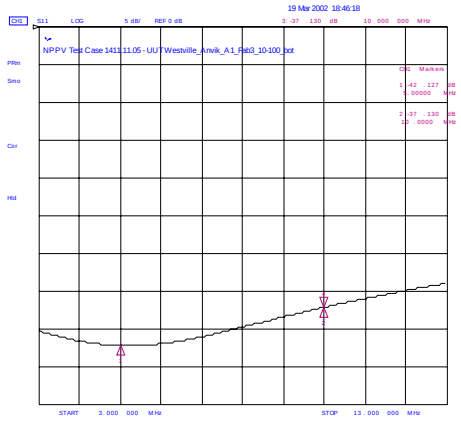


2. Adjust the spectrum analyzer to the following settings.

Table 20-1. Analyzer Configuration for RD Circuit Differential Input Impedance

Start Frequency	3 MHz
Stop Frequency	13 MHz
Resolution BW or IF BW	Lowest practical bandwidth supported by equipment in the range of 10 KHz to 200 KHz.
Number of Points (Resolution)	Maximum for instrument (≥ 401)
Acquire	Average (if necessary)
Vertical Division	10 dB/division
Mode	Network Analyzer

3. Ensure the UUT is in 10 Mbps mode.
4. Perform a calibration on the S11, S-parameter, port and turn correction on.
5. Use the 50 Ω load to verify the calibration. The return loss should fall in the range of 9.5 dB and 9.6 dB.
6. Set the marker to the worst-case return loss between 5 MHz and 10 MHz inclusive.



7. Record the amplitude (dB) of the return loss.
8. Ensure the value falls within the specification.

Appendix A ST.exe User Guide

A.1 Getting Started

1. The following items are required:
   - — ST.exe revision 5.10 or later
   - — 82558 based NIC/LOM
   - — Computer with one available PCI slot (for use with a NIC) capable of booting under DOS
2. While the computer is off, install the NIC in a PCI slot (if applicable).
3. Turn the computer on, then copy the 000880.PAT pattern file to the same directory as ST.exe on the computer's hard drive (alternatively, run ST.exe from a bootable floppy disk).
4. Change to the directory where ST.exe is located.

A.2 Using ST.exe

1. At the DOS prompt, type "ST" and press <Enter>.
2. A light colored screen should appear with several text items at the top of the screen. The text items are the option menus. At the top left of the screen, "PCI Device" should be highlighted. Press <Enter>. (If "PCI Device" is not selected, highlight it using the left or right arrow key.)
3. Use the up or down arrow key to select the line that reads "PCI D101 NIC".

Note: This name may be different for future product steppings. Choose the name that describes the NIC or LOM solution under test.

4. Under the "PCI Device" menu, "Initialize" should be highlighted. Press <Enter>. (If "Initialize" is not selected, highlight it using the left or right arrow key.)
5. A menu should appear with the following options:

   ```
   Auto
   Setup 100
   Setup 10
   Exit
   ```

6. Use the up or down arrow key to select "Setup 10" for 10 Mbps operation, or "Setup 100" for 100 Mbps operation. Press <Enter>, then press Escape to go back to the main menu choices.

Note: ST.exe does not confirm that a change has been made.

A.3 Quitting ST.exe (Returning to DOS)

1. Press <Escape> until only the top-most menu is available.
2. Use the left or right arrow key to select "Exit".
3. Press <Enter>. The program should exit and return to the DOS prompt.

A.4 Reading and Saving Register Contents

1. Select the desired menu from the main drop down list.
2. Press R (or the appropriate number/letter located under each column) to read the register contents.
3. Use the arrow keys to select the desired register function.
4. Press <Enter> to toggle to the desired state.
5. Repeat steps 3 and 4 until all register fields display the desired settings.
6. Select the number of the “Write” under the column where the changes were made.
7. Select “Read All” to verify changes were accepted.
8. After reading the registers to confirm the change(s), press <Escape> until the main menu reappears.

A.5 Finding ST.exe Settings for 100Base-TX Testing

The following table assumes the correct chip has already been selected from the “PCI Device” menu.

Table A-1. ST.exe Settings and Default Values

Setting Number	ST.exe Setting	Location	Default Value
1	Force 100	Initialize → Setup 100	Auto
2	Force Good Link	MII → Phy Ext Capability → Command	Normal (Norm)
3	Data Scrambling	MII → Phy Ext Capability → Command → Status Regs → Scrambler	Enable (Ena)
4	4b/5b Encoding	MII → Phy Ext Capability → Command → Status Regs → Bypass 4b5b	Normal (Norm)
5	3/4 Encoding	MII → Phy Ext Capability → Command → Status Regs → Force 3/4	Normal (Norm)
6	Duplex	MII → Phy Ext Capability → Cmd & Status → Duplex Mode	Half Duplex (HD)
7	Transmit Packet Size	Transmit → Setup → Packet Size	1024 bytes
8	Transmit Threshold	Transmit → Setup → XMIT Threshold	1024 bytes
9	Transmit Pattern File	Transmit → Setup → XMIT Pattern	Fixed
10	Promiscuous Mode	CSMA/CD → Config → Promiscuous	Disable
11	Save Bad Frames	CSMA/CD → Config → Save BF	Enable
12	Packet Sequence Numbers	Transmit → Setup → Pkt Seq Numbers	Disable
13	Broadcast	CSMA/CD → Config → Broadcast	Enable

Note: It is possible to reset the 82558 without having to reboot the system. Select MII Æ Phy Base Regs Æ Cmd & Status Æ Reset.

A.6 Creating User-Specified Pattern Files

For ST.exe to transmit user-specified patterns, pattern files with a “.PAT” extension must be in the same DOS directory as ST.exe. Pattern files are ASCII files consisting of hexadecimal bytes separated by carriage returns.

Example A-1.Creating the 55.PAT File

Use a text editor to create the 55.PAT ASCII file for repeating binary data bytes of 0101 0101 (hexadecimal 55).

1. Name the file 55.PAT.
2. The file will contain between 64 and 1518 lines. Each line will consist of the number “55”.

In other words, the file will look like this:

55

55

55

55

55

55

Repeated between 64 and 1518 times.

3. Make sure to save the file as plain ASCII.

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Appendix B Parts and Suppliers

Most of the parts used in the test fixtures listed in Appendix C, “Test Setups” can be built using standard, high quality parts. The following list provides suppliers and part numbers for parts that may be non-standard.

B.1 Baluns

North Hills Wideband Balun Transformers: NH13734 (need 3 per test kit).

B.2 Male RJ-45

- Digi-Key, Newark, or Inmac
- AMP

B.3 Shielded Female RJ-45

- Newark Electronics
- Molden
- AMP

B.4 High Quality CAT5 Cable (not stranded or CAT5 Patch Cable)

- Newark Electronics
- Belden DataTwist™ Five
- AT&T
- General Cable
- Black Box Corp
- Inmac Clear Signal™
- Lucent SystiMax™

B.5 BNC to Hook Clip Adapters

- Digi-Key
- Newark

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Appendix C Equipment List

The following list of test equipment may meet the requirements necessary to provide accurate results for 100Base-TX ANSI TP-PMD PHY conformance testing. Intel makes no guarantees that this equipment will produce the desired results.

C.1 Network Analyzers / Test Sets[1]

- HP4396B Network/Spectrum Analyzer

HP85046A S-Parameter Test Set

- HP4195A Network Analyzer

HP41952A Test Set

C.2 Digitizing Oscilloscopes / Differential Probes[1]

- Tektronix TDS 784 Series Digitizing Oscilloscope
- Tektronix DSA 602A Digitizing Signal Analyzer
- Tektronix P6247 High Bandwidth Differential Probe

C.3 Function Generator

- HP 8116A Pulse/Function Generator

1. Trademarks are the property of their respective owners.

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Appendix D Test Setups

D.1 Test Setup 1

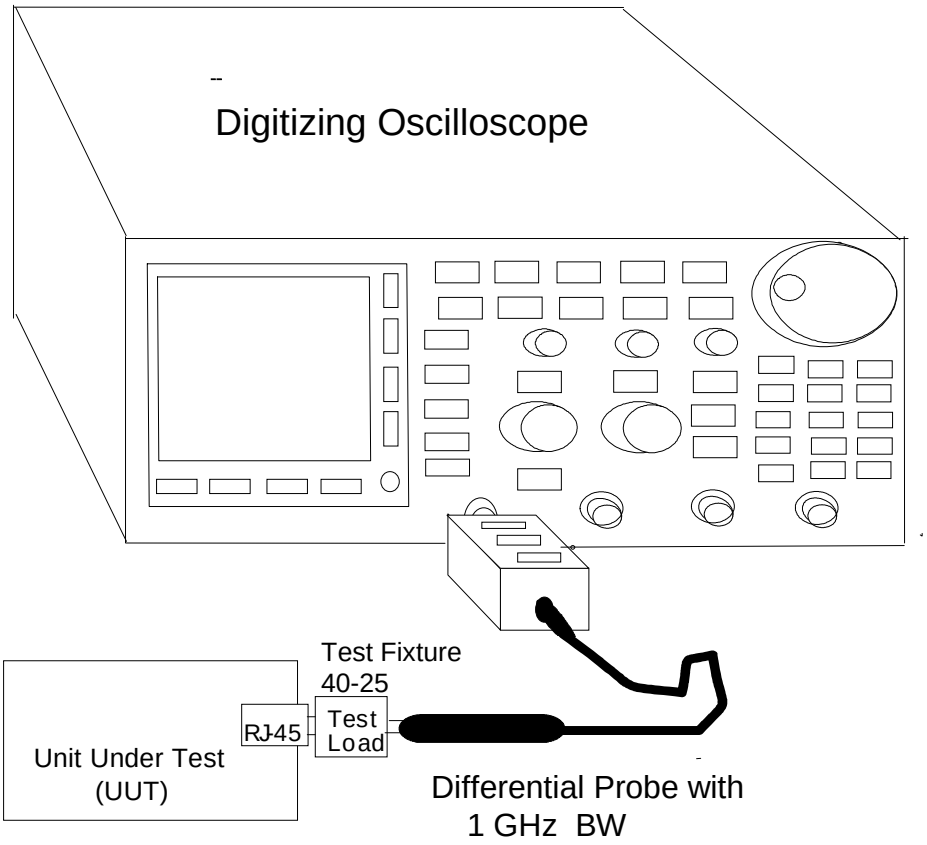

Figure D-1. Test Setup 1 (Specifications: 40.6.1.2.1 and 40.6.1.2.2)

D.2 Test Setup 2

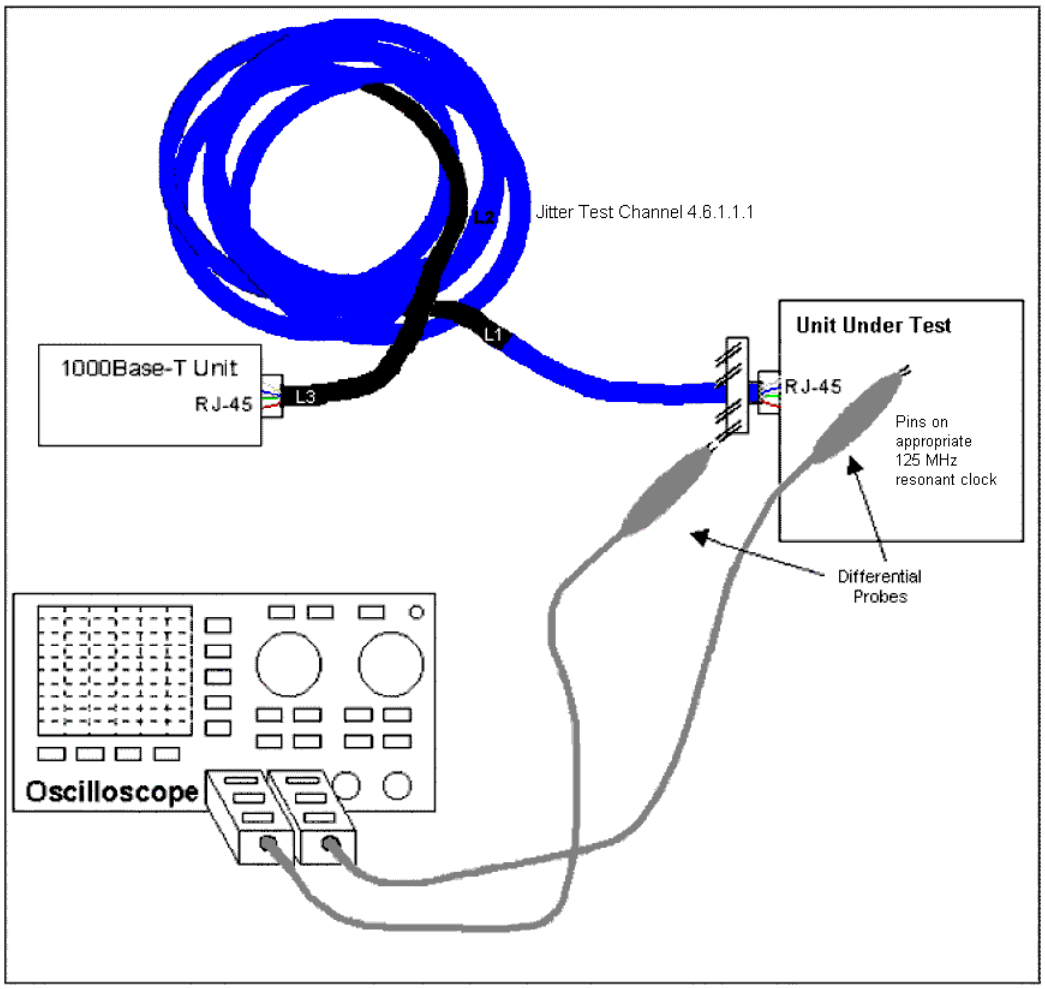

Figure D-2. Test Setup B (Specification 40.6.1.2.5)

UUT Preparation Notes

The Unit Under Test (UUT) must be able to operate in the four specified test modes and in master and slave modes. The UUT must also be able to transmit and receive Ethernet data frames.

Test pins are required for some of the tests on a 125 MHz transmit clock signal. Sources of 125 MHz clocks will vary on different boards. On some boards and systems, the source clock (and oscilloscope trigger signal) will be a 125 MHz oscillator or a 125 MHz GMII transmit clock coming from MAC layer silicon. Some boards provide a test pin(s) that allows internal clocks to be exposed for testing purposes. By using register settings, the appropriate 125 MHz clock can be exposed. A 125 MHz clock source may not be available on some boards. In this instance, a 25 MHz source clock used by the PHY unit to derive its internal clock may be used.

D.3 Test Setup 3

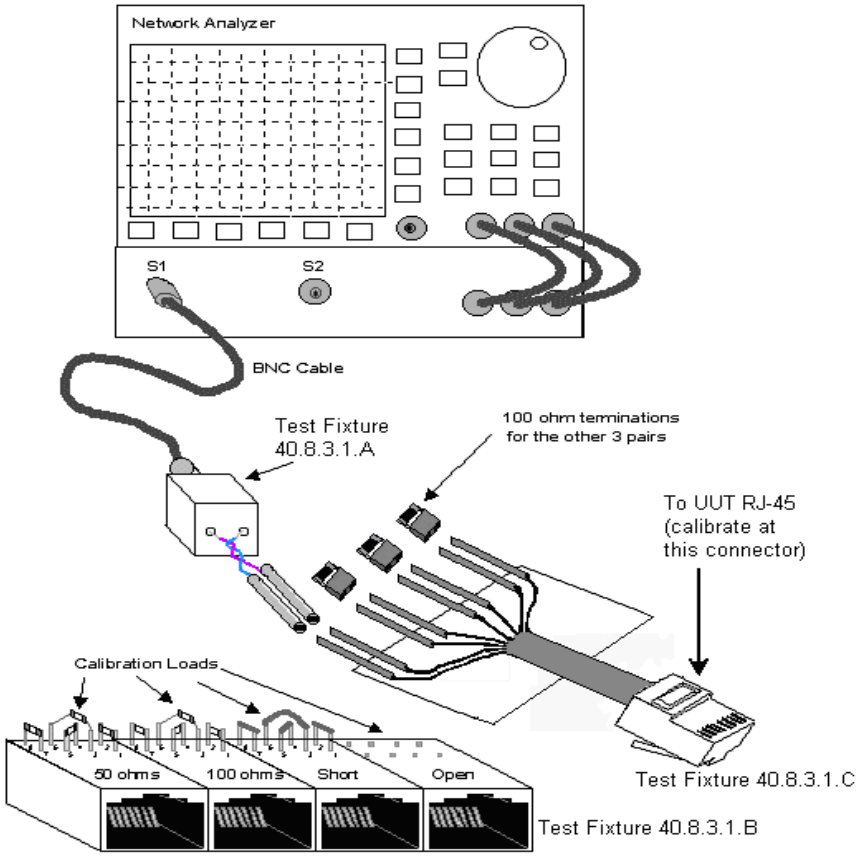

Figure D-3. Test Setup E (Specification 40.8.3.1)

Note: The small fixture, with square pins and a male RJ-45, that plugs into the UUT's RJ-45 connector can be replaced by a short cable with square pins and a male RJ-45 connector.

D.4 Test Setup 4

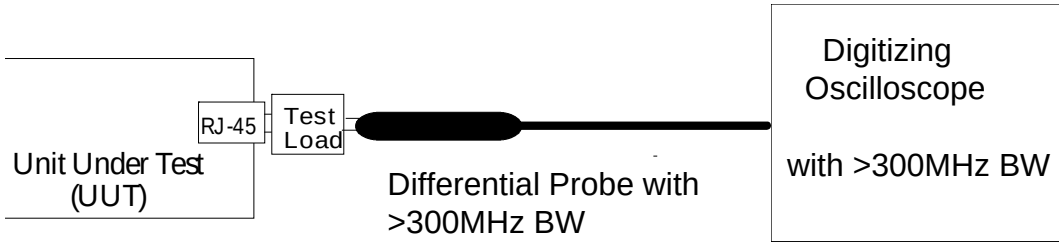

Figure D-4. Test Setup 4

D.5 Test Setup 5

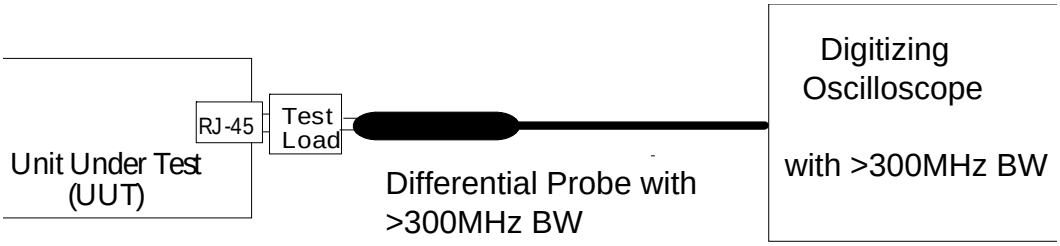

Figure D-5. Test Setup 5

D.6 Test Setup 6

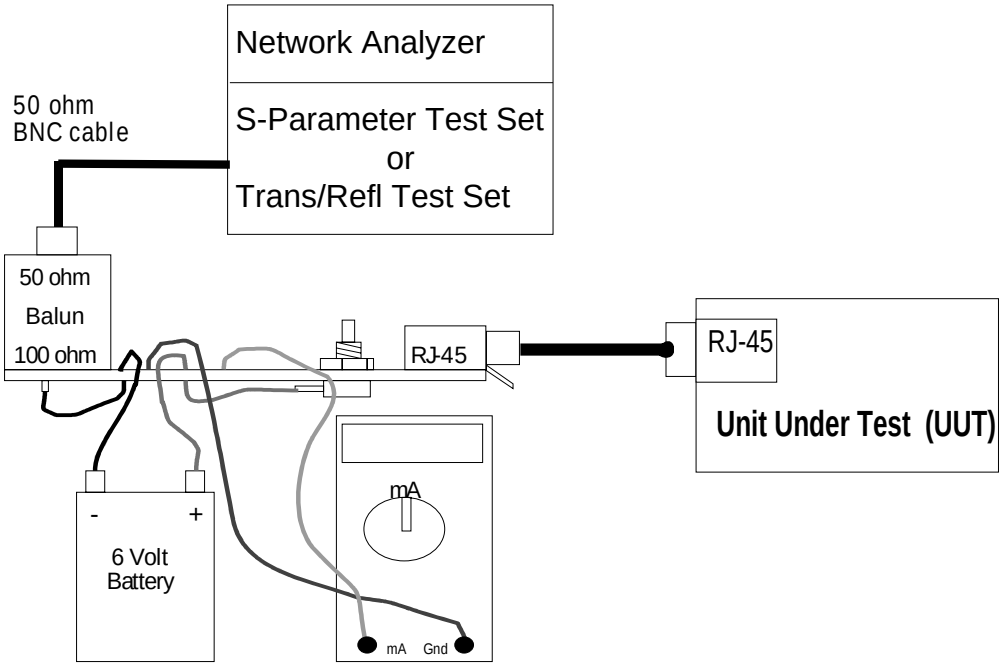

Figure D-6. Test Setup 6

D.7 Test Setup 7

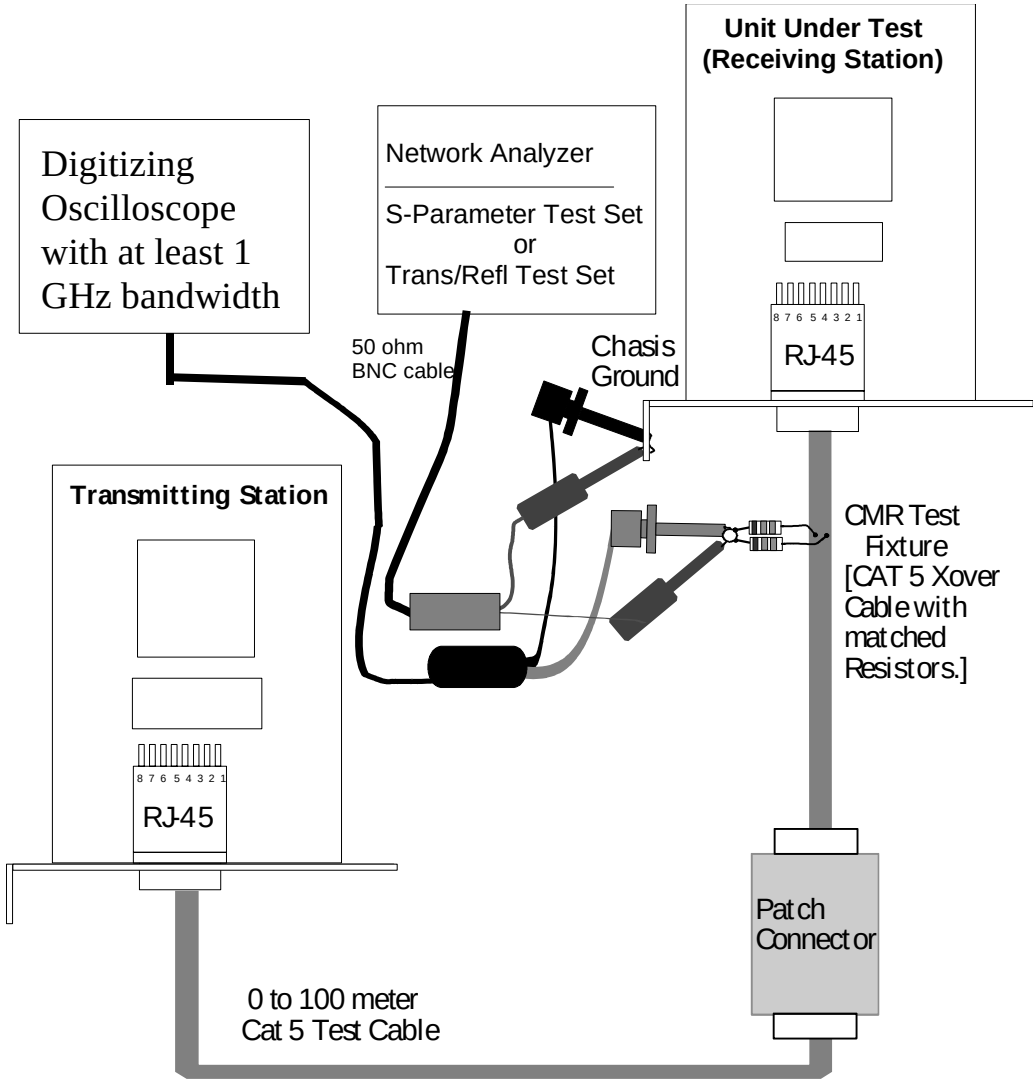

Figure D-7. Test Setup 7

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Appendix E Test Fixture Construction

E.1 General Test Fixture Construction Guidelines

1. Unless otherwise specified, always use solid 22 AWG wire or solid 24 AWG wire. Ideally, the wires for differential test fixtures can be taken from a scrap piece of high-quality, solid-conductor, Category 5 cable.
   - — Keep both sides of each differential pair balanced.
   - — Keep lead lengths the same on each side of each differential pair.
   - — Route both leads, within a differential pair, next to each other.
   - — Center resistors and other components that are soldered between differential pairs between the pair of wires or traces.
   - — Match values and lengths as closely as possible when two of same value components are shown in an illustration.
2. Always keep lead lengths as short as possible, without violating the rules listed under the second bullet in guideline 1 (above).
3. If the differential leads on a test fixture need to be more than one or two inches long and if possible, twist the two leads (of the differential pair) around each other.
4. Tightly toleranced components should be used wherever possible.
   - — When using an ohm meter to choose the best resistor values, subtract the meter's lead resistance from the measured resistance values.
   - — As a starting point, resistors should be 1% or better tolerance. Use an ohm meter, and select resistors that are within 0.1 Ω of the required value. When a pair of the same value is used, they should be matched within 0.1 W before soldering, and within 0.2 Ω after soldering. If an illustration shows a tighter tolerance, follow the illustration.
   - — Capacitors should be 5% or better tolerance. When a pair of the same value is used, they should be matched as close as possible. If an illustration shows a tighter tolerance, follow the illustration.
   - — Inductors should be 10% or better tolerance. When a pair of the same value is used, they should be matched as close as possible. If an illustration shows a tighter tolerance, follow the illustration.
5. Each test fixture and cable should be labeled with its function and identity.
6. When using twisted pair Ethernet cable to build test fixtures (or very short test cables), use solid conductor Category 5 cable. The impedance is better controlled than Category 5 patch cable and Category 3 cable. Also, solid conductor Category 5 cable has lower insertion loss.

E.2 RJ-45 Connector Pin-Out and Ethernet Cable Wire Assignment

- Pin 1 is channel A+, white/orange wire
- Pin 2 is channel A-, orange wire
- Pin 3 is channel B+, white/green wire
- Pin 6 is channel B-, green wire
- Pin 4 is channel C+, white/blue wire

- Pin 5 is channel C-, blue wire
- Pin 7 is channel D+, white/brown wire
- Pin 8 is channel D-, brown wire

Table E-1.

Contact (pin)	Straight Through Cable	Crossover Cable
1	A+ to A+	A+ to B+
2	A- to A-	A- to B-
3	B+ to B+	B+ to A+
4	C+ to C-	C+ to D+
5	C- to C+	C- to D-
6	B- to B-	B- to A-
7	D+ to D+	D+ to C+
8	D- to D-	D- to C-

E.3 Building and Testing UTP LAN Cables to Insertion Loss Specifications

The ANSI TP-PMD specification requires the use of “standard” test cables to perform common-mode rejection and standard bit error rate tests. In Annex A.1.1 of the ANSI standard, the TP-PMD partially defines these cables by their intended insertion loss, rather than their physical length. (For a list of required cables, see Table D-1. For more detail, read the TP-PMD.)

The insertion loss of the test cables must be characterized by measurement. Do not assume 1.0 dB of loss per 10 meters of CAT 5 cable. Almost all CAT 5 cable is either much lower in loss, or significantly higher. Because the cables are not consistent, measure the characteristic insertion loss of the appropriate type of cable, cut it to length (the length that provides the desired loss), and add connectors.

E.3.1 Purpose

This section explains a general method of measuring the insertion loss of twisted pair Ethernet cable, and how to calculate the desired cable length based on a target insertion loss. This section is not an exhaustive treatment of this topic, nor is it a replacement for a network analyzer’s instruction manual.

E.3.1.1 Network Analyzer Setup and Calibration

Measuring a cable with a network analyzer is relatively straightforward. A vector network analyzer is more accurate than a scalar network analyzer. Use two 50 ohm unbalanced to 100 ohm balanced transformers to match the cable impedance with that of the network analyzer. (North Hills Balun model NH13734 is okay, and so is Model 0300BB).

1. Connect the 50 Ω side of one balun to port one on the network analyzer via a BNC cable.
2. Connect the 50 Ω side of the other balun to port two of the network analyzer through a second BNC cable. See Figure D-1.
3. In two-port or S21 (insertion loss) mode, set the network analyzer's start frequency to 1 MHz, and the stop frequency to 101 MHz (If your analyzer or baluns are BW limited, calibrate to a little over 16 MHz instead of to 101 MHz).

4. Set the analyzer's display format to insertion loss in dB.
5. Perform a two-port calibration (Through connect & Isolation):

Note: Two port calibration methods may vary for different network analyzers. Refer to the equipment's users manual for more details.

a. For the through connect, connect the 100Ω side of one balun to the 100Ω side of the other balun via a very short CAT5 twisted pair cable.

b. For the isolation measurement, terminate each balun's 100Ω side with a 100Ω resistor.

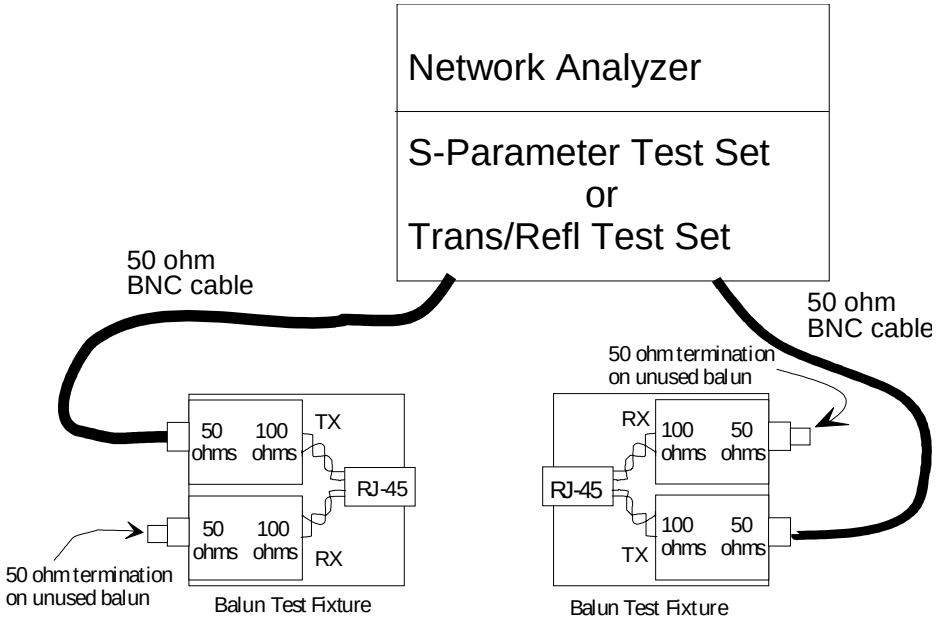


Figure E-1. Network Analyzer Setups for Calibration and Measurement of Insertion Loss

6. Turn correction on.
7. Set triggering to continuous sweep.
8. Put a marker on 16 MHz.
9. After calibration, check the calibration quality by measuring the two calibration standards.

a. Reconnect the short CAT5 through cable between the two baluns. Insertion loss should be zero dB. Most network analyzers should be capable of zero dB within +/- 0.05 dB or less.

b. Put the 100 ohm resistor loads back on each balun. The insertion loss (isolation) should be greater than 40 dB (On many network analyzers, isolation will be > 60 dB).

Note: Treat all loss and isolation levels as absolute values. If your analyzer displays an isolation/insertion loss of -65 dB, it is actually 65 dB, unless you are measuring an amplifier or a device with greater than unity gain (i.e. negative loss = gain).

E.3.1.2 Measuring the Insertion Loss of the Twisted Pair Cable

10. Connect a known length (preferably 50 meters or more) of the twisted pair cable between the two baluns' 100 ohm sides (Connect the network analyzer to the cable's TX pair: orange & orange/white at both ends).
11. Record the insertion loss value for the marker at 16 MHz. The analyzer in should be in continuous sweep mode.
12. Recalibrate if required, and measure the cable's RX insertion loss (green & green/white).
13. Divide the insertion loss at 16 MHz by the length in meters. The result of this calculation is the characteristic dB/meter. It is not uncommon for TX cable loss and RX cable loss to be slightly different. Average the numbers to calculate a single insertion loss/meter for the cable.
14. To calculate the length of cable for a required insertion loss, divide the required insertion loss by the loss/meter.
15. Build cables to the length(s) that you calculated .
16. Repeat steps 10 through 14 to measure the TX and RX insertion loss of the cables that were built in step 15.

E.3.2 Alternate Insertion Loss Measurement Techniques

Cable insertion loss can also be measured/calculated by more difficult and/or less accurate methods:

- Signal generator, two baluns, and a couple of power meters.
- Signal generator, two baluns, and an oscilloscope with one or two differential probes (in lieu of one or both power meters).

Note: A variation on the last method dispenses with the baluns and the differential probes, but requires the use of two (matched) channels on the oscilloscope, two phase-matched coaxial cables, and a signal generator.

All of the alternative measurements require the user to manually add or subtract some correction factors, and/or convert from voltage to decibels in order to obtain the cable's insertion loss.

Note: A network analyzer is more accurate than the alternate measurement methods.

Table E-2. Test Cables 1-5

Test Cable	Type	Insertion Loss	Frequency	Error
1	CAT5	0.5 dB	16 MHz	± 0.20 dB
2	CAT5	2.5 dB	16 MHz	± 0.20 dB
3	CAT5	5.0 dB	16 MHz	± 0.20 dB
4	CAT5	7.5 dB	16 MHz	± 0.20 dB
5	CAT5	10.0 dB	16 MHz	± 0.20 dB

E.4 Other Test Fixtures

E.4.1 Fixture 40-25

Test fixture 40-25 is used for Output Level and Level Accuracy. It terminates each channel with a 100-ohm load. Each Resistor is 100 Ω ±0.1 Ω. A 100 Ω resistor across all four MDI signals must be present at the same time.

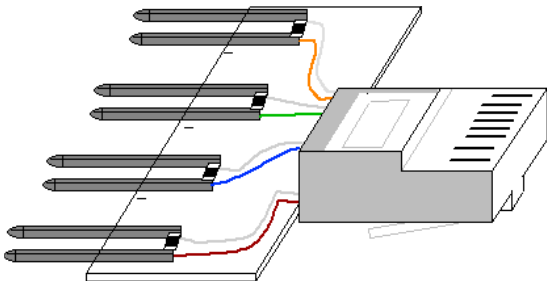


Figure E-2. Angled side view

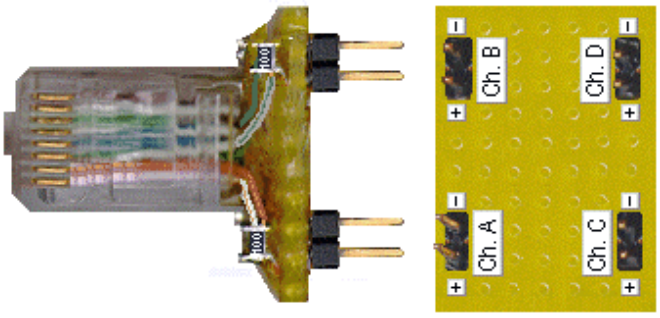


Figure E-3. Side and end view

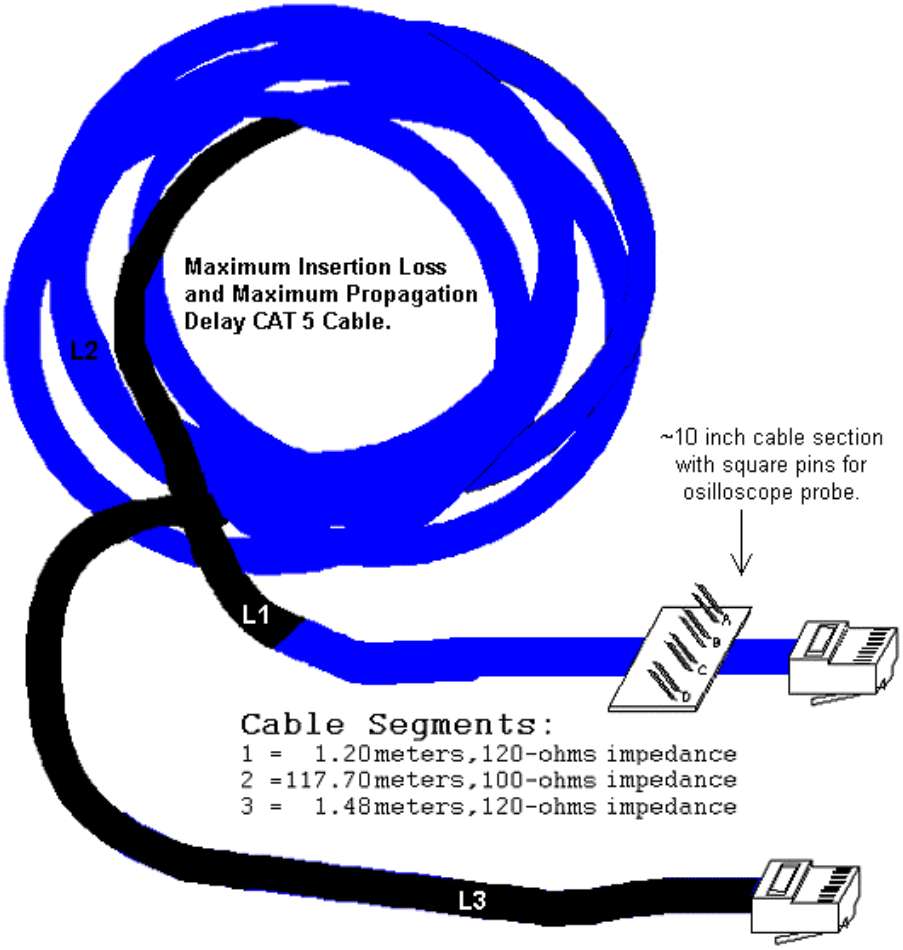
E.4.2 Fixture 40.6.1.1.1.A Differential Breakout Cable (Jitter Test)

A short cable is required for the transmitter jitter test and for the alien crosstalk tests. It is connected to the end of long test cables by using a CAT 5 patch connector and is approximately 10 inches in length. It is a CAT 5 cable with four pairs of square test pins, with one pair on each differential pair within an inch of one of the male RJ-45 connectors.

E.4.3 Fixture 40.6.1.1.1 Test Cable

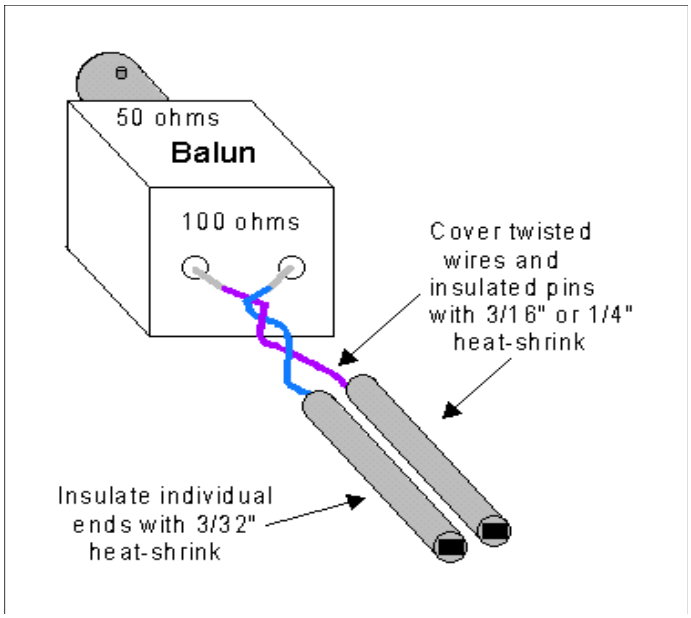
This cable is used for master and slave transmit jitter (IEEE 802.3ab, Section 40.6.1.2.5) and alien crosstalk noise rejection (IEEE 802.3ab, Section 40.6.1.3.4). It is made from three segments as defined in IEEE 802.3ab, Section 40.6.1.1.1.

There are two segments with 120-ohm characteristic impedance, and one long CAT 5 cable section with 100-ohm characteristic impedance. Near the UUT end of this cable, fixture 40.6.1.1.1.A (above) is attached.



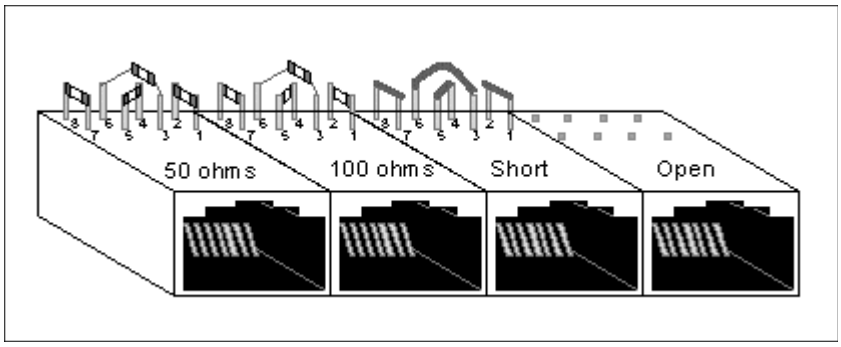
E.4.4 Fixture 40.8.3.1.A

Fixture 40.8.3.1.A is a Balun test fixture. A North Hills NH13732 or similar balun should be used.



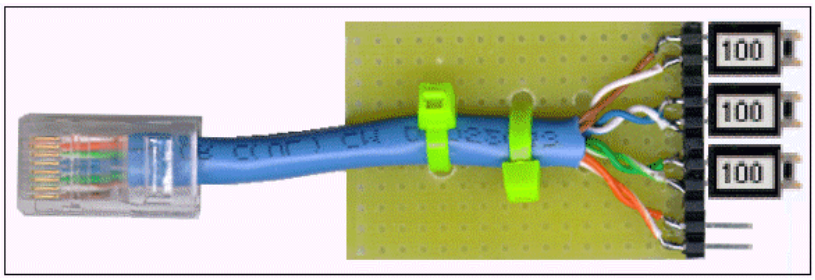
E.4.5 Fixture 40.8.3.1.B

Fixture 40.8.3.1.B is also used for MDI return loss. The illustration shows the network analyzer calibration loads.



E.4.6 Fixture 40.8.3.1.C

Fixture 40.8.3.1.C is a square pin fixture for MDI return loss. It allows a single Balun to test all 4 channels.



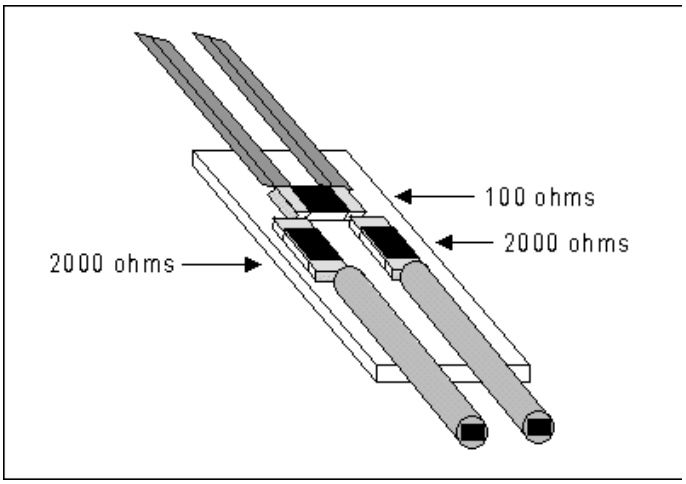
The short CAT 5 cable with four pairs of square pints mates to the Balun test fixture for return loss tests. 100-ohm resistor loads are installed on the channels that are not being tested.

E.4.7 Fixture 40-28A

Fixture 40-28A is used for the alien crosstalk noise rejection test. It requires one-half meter long CAT 5 cable with female test pins on the transmit differential (positive and negative) pins at one end. The transmit differential pins correspond to the orange and orange-white twisted cable pair in the CAT 5 cable.

E.4.8 Fixture 40-28B

Fixture 40-28B is also used for the alien crosstalk noise rejection test.



E.4.9 Fixture 40-32

Fixture 40-32 is used to test common-mode output voltage and is required for IEEE 802.3ab, Section 40.8.3.3. A schematic for fixture 40-32 can be obtained in the IEEE 802.3ab specifications.

A 47.5-ohm resistor is soldered to the end of each wire on each differential pair. At the opposite ends, each pair of 47.5-ohm resistors is soldered together. Where the 47.5-ohm resistors are soldered together, they are also both soldered to one of the square pins in the top row. All of the 47.5-ohm resistors, and all of the top-row square pins are insulated from the copper ground plane by a layer of kapton tape. The bottom row of right-angle square pins are soldered to the copper ground plane (diagram below shows the four solder joints in the bottom view just below “Output V” on the label). The shield on the RJ-45 connector is soldered to the fixture’s copper ground plane.

Note: On the top-side, each top row square pin has a 49.9 ohm resistor soldered to it, which is not visible. The other end of each 49.9-ohm resistor is soldered to the corresponding ground pin in the bottom row of square pins.

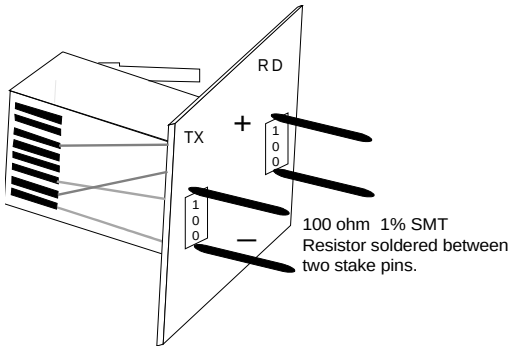
Another way to visualize the how the resistors are arranged:

On each test channel, two 47.5-ohm resistors and one 49.9-ohm resistor form a “Y.” A top-row square pin is soldered to the center of the “Y.” The top-row square pin is soldered to all three resistors, at this single point on the “Y.” The opposite end of the 49.9-ohm resistor is soldered to a ground pin. Kapton tape insulates the top-row square pins and the 47.5-ohm resistors from ground.

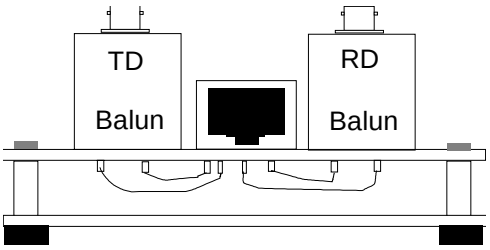
Note: Fixture 40-32’s copper tape ground plane is soldered directly to the metal shield on the RJ-45. The fixture’s RJ-45 shield connects to the UUT shielded connector. The lower row

of test pins are all connected to the UUT chassis ground (indirectly) through the fixture's copper ground plane.

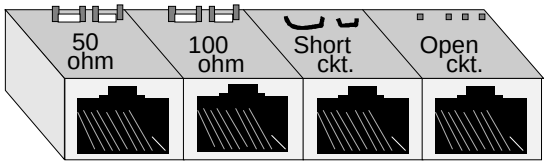
E.4.10 100 Ohm UTP Test Load



E.4.11 100Base-TX Balun Test Fixture



E.4.12 Network Analyzer Calibration Fixture



Four, female RJ-45 connectors, glued to each other.

Open ckt. - Cut pins flush to the

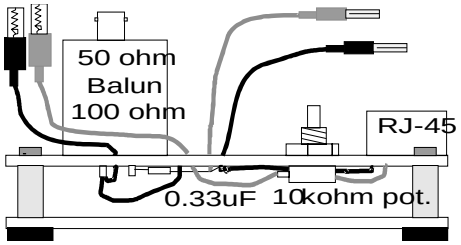
Short ckt. - Tie pin 1 to pin 2. Tie pin 3 to pin 6. Cut off the

100 ohm - Solder 100 ohm SMT resistors between: pin 1 and pin
and between pin 3 and pin

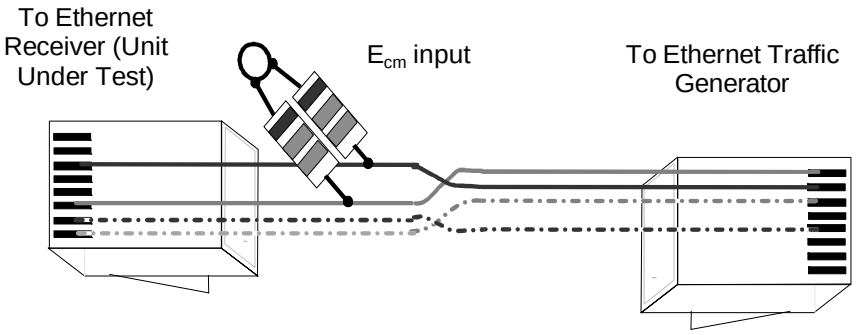
50 ohm - Solder 50 ohm SMT resistors between: pin 1 and pin
and between pin 3 and pin

Load Fixture for Network Analyzer Calibration

E.4.13 Open Circuit Inductance Test Fixture



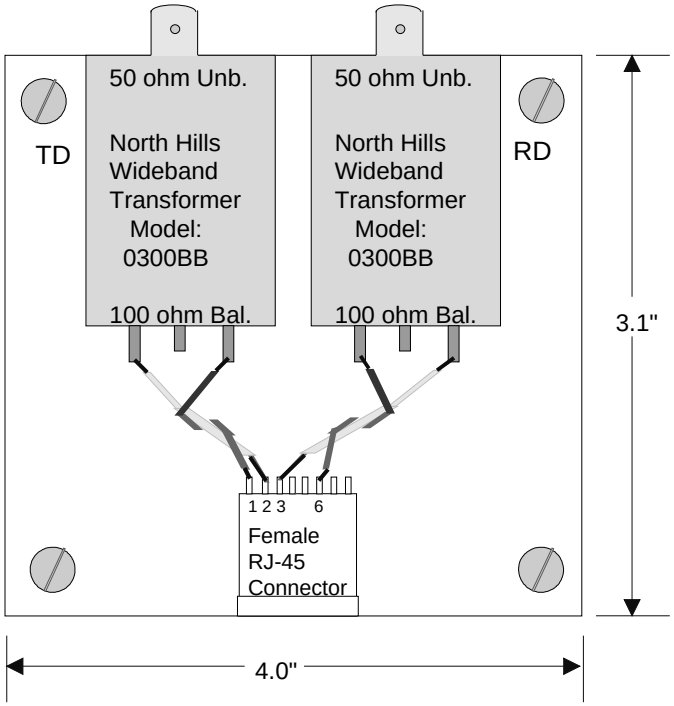
E.4.14 Receiver Common-Mode Rejection Test Fixture



Receiver Common-Mode Rejection Test cable with two identical value resistors
$R_1 = R_2$, and $449\Omega \leq R \leq 560\Omega$

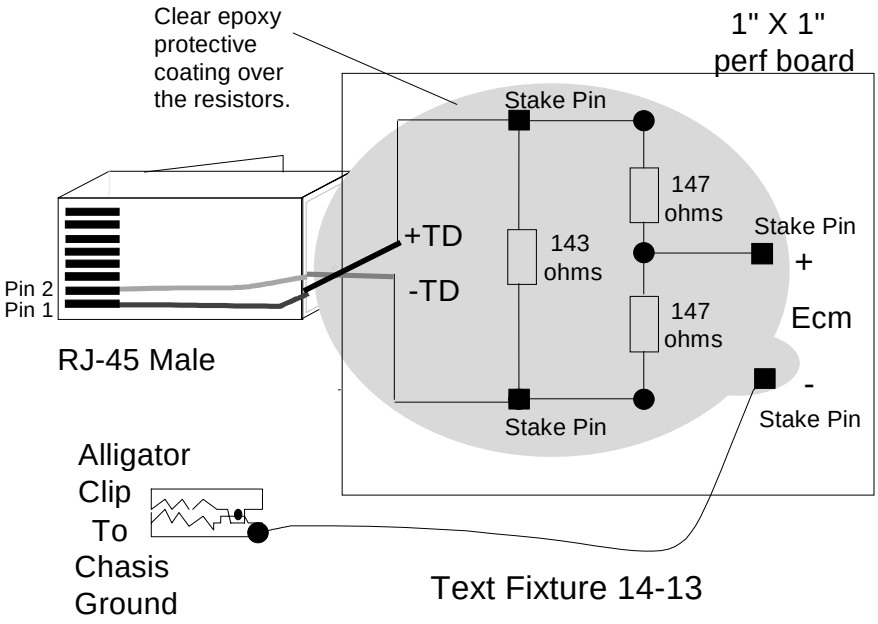
Note: Each Resistor must be soldered an equal distance from the end of the RJ-45 connector (i.e. both sides of the receive signal path must be symmetric). Also, the wires in each pair must be ***twisted*** CAT5 wire (to make the signal path clear, the illustration does not show twists, but the real fixture must have twisted wires in each differential pair).

E.4.15 10Base-T Balun Test Fixture



10Base-T Balun Test Fixture, Top View

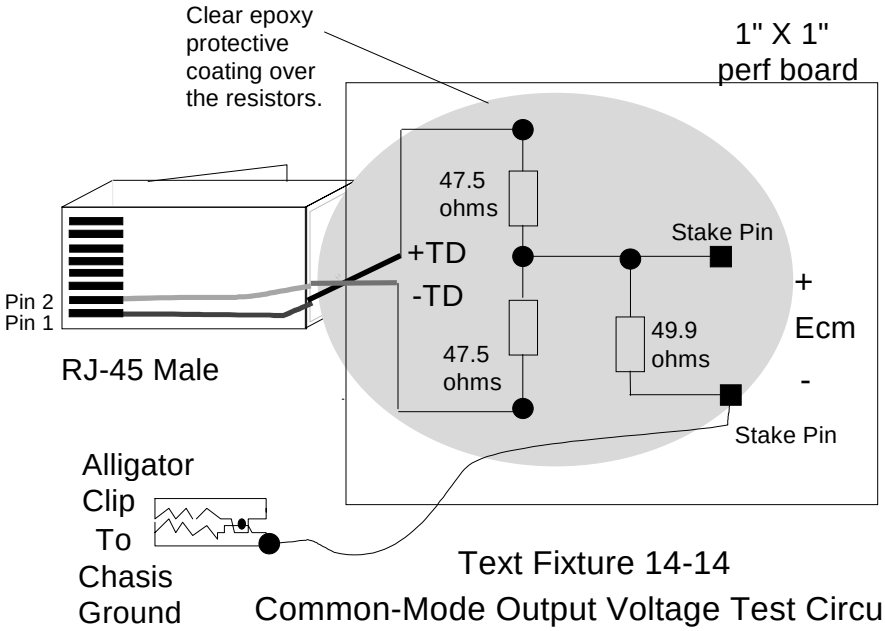
E.4.16 Common-Mode Output Voltage Test Circuit (Fixture 14-14)



Text Fixture 14-13

Transmitter Impedance Balance and Common-Mode Rejection Test Circuit

(Used for Test Cases 1411.10.08 and 1411.10.10)



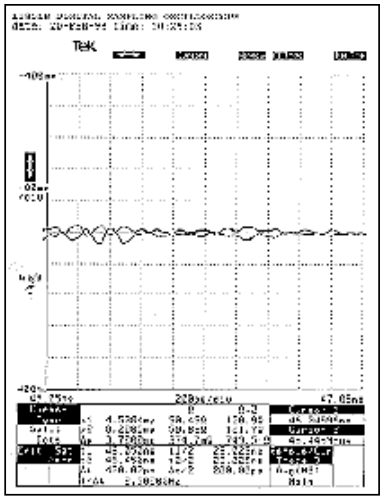
Text Fixture 14-14

Common-Mode Output Voltage Test Circuit

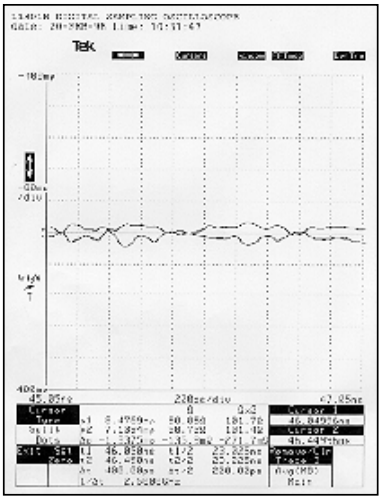
(Used for Test Case 1411.10.09)

Appendix F Reducing Measurement Error by Avoiding Cable Bending

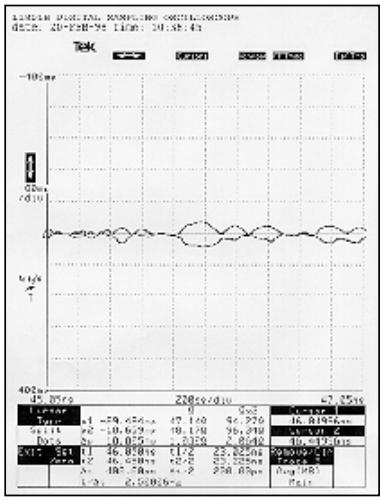
Sharp bends can change the impedance of twisted-pair cables. The following scope displays show the results of bending approximately 1 meter of CAT5 Twisted-Pair Cable connected to a differential TDR plug-in on a Tektronix 11801 oscilloscope. Split Dot Cursor positions are fixed at the fifth and seventh graticles (cursors at 23.025ns and 23.225ns).



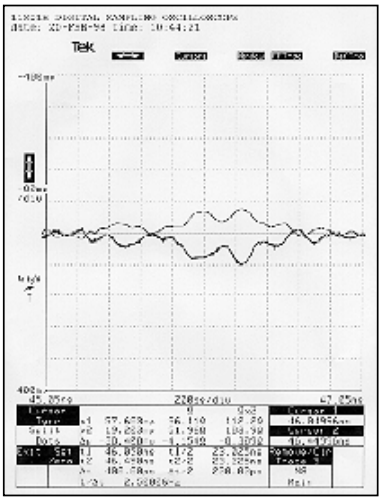
Cable Straight
Cursor 1 = 100.9 Ω
Cursor 2 = 101.7 Ω



Cable with 2" diameter loop in cursor area.
Cursor 1 = 101.7 Ω
Cursor 2 = 101.4 Ω
Note: A gentle bend has little affect.



Cable with half-knot in cursor area.
Cursor 1 = 94.3 Ω ; Cursor 2 = 96.3 Ω
Lower Z is caused by dielectric compression (Conductors are closer together).



Half-knot is untied & straightened.
Cursor 1 = 112.2 Ω ; Cursor 2 = 103.9 Ω
Higher Z is caused by "bird cage" effect (Conductors are farther apart).

$$Z_0 = \frac{276}{\sqrt{Er}} LOG \frac{2D}{d}$$

Figure F-1. Equation for Twin-Lead (Twisted Pair) Cable

$$Z_0 = \frac{138}{\sqrt{Er}} LOG \frac{D}{d}$$

Figure F-2. Equation for Co-axial Cable

Using the Twin-Lead equation for the CAT5 cable shown in Figure E-1, we can calculate the effect of compressing the cable (during sharp bends) or separating the wires (straightening after a sharp bend).

By compressing the dielectric between the two wires by 0.002 inch, the cable impedance was decreased to 95.3 ohms at the point of compression. This is similar to the impedance produced by the knot.

By separating the wires in the pair by 0.003 inch, the cable impedance increased to 111.9 ohms at the point of separation. This is similar to the impedance produced when a kinked cable is straightened. The wires can “birdcage” or separate.

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Appendix G Troubleshooting Guide

Many problems can occur during PHY conformance testing relating to problems with the equipment and software as well as with the Unit Under Test. This section provides troubleshooting tips to help debug these problems.

G.1 Test Problems

The most common problems which occur during testing involve displaying waveforms. Familiarity with the scope being used will greatly reduce the problems in this area. Refer to the scope's user's manual for more information. Most other problems are caused by the test setup and software configuration.

Some of the steps below may not be applicable to all of the procedures. Use only the ones that make sense for the test being performed.

G.1.1 Oscilloscope Setups

- Make sure all test equipment meets or exceeds the specifications listed in the introduction to this manual.
- Confirm that the expected voltage range of the signal does not exceed the capabilities of the differential probe being used. The probe listed in Appendix B requires the attenuation to be turned on in order to perform the measurements correctly.
- Confirm that the correct channel has been selected on the scope. Also confirm that the correct channel has been selected to be triggered on.
- Verify that the test fixture(s) and scope are connected as shown in. Make sure the scope probe is connected to the test fixture with the correct polarity.
- Check that the host computer for the UUT has been booted under DOS, and that LANConf.exe is running.
- Confirm that the UUT has been forced into 100Mbps mode. Once this has occurred (and before any other settings have been changed) scrambled MLT-3 waveforms should appear on the scope display. If the scope has a feature to automatically adjust scope settings, use it to make sure a signal is present. If no signal appears, power down the computer, unplug it, plug it back in, and restart it. Start LANConf.exe and force the UUT into 100Mbps mode.
- Check all LANConf.exe settings listed in the test procedure. Many problems are caused by simply forgetting to "Write" a change to memory. In order to make a change to a register value in LANConf.exe, it is necessary to first "Read" the relevant register values, "Write" the changes, and finally "Read" to confirm that the changes have been made. Make sure that the correct "Write" is used, as there may be more than one per screen.
- Do not use the automatic measurement features on the scope (if available). These features often do not correctly measure the desired waveform characteristics and as such are unreliable.

G.1.2 Network Analyzer Setups

- Make sure all test equipment meets or exceeds the specifications listed in the introduction to this manual.

- Verify that the analyzer is in “Network Analyzer” mode if it is a Spectrum/Network Analyzer.
- Make sure that the test equipment has been configured as shown in the test procedure.
- Check that the test fixtures have been connected as shown in Appendix B.
- Make sure the host computer is on and LANConf.exe is running. Although it may appear that the test can be done with the unit off, it does not always provide the same results. The only valid results are those that are taken when the UUT is powered up and LANConf.exe has been configured.
- Recalibrate the network analyzer as described in the test procedure. After calibration, confirm that the 50 ohm load shows a return loss of 9.54 dB. Also verify that the open and short loads produce the expected results.
- Check the cables connecting the network analyzer to the test fixture, and the test fixture to the UUT. If the analyzer reading changes noticeably when any of the equipment is moved (especially the coaxial cable) the cabling or fixture may need to be replaced.

G.2 Conformance Problems

Several factors can cause boards to fail PHY conformance testing. The best way to prevent failure is to follow Intel’s reference schematic and board layout guidelines which can be found in the product design kit.

Many of the tests described in this document deal with the transmitter characteristics. If the transmitter fails to meet specification, the link partner’s receiver may fail to correctly receive the signals, resulting in high Bit Error Rates on the receiving unit.

G.3 Differential Output Voltage (UTP) (ANSI specification 9.1.2.2)

This is one of the more important tests conducted during PHY conformance testing. If the design exhibits output voltage that is too high, the networking subsystem will, most likely, not pass FCC and EN55022 emissions testing.

In a networking environment, a system with this condition would not be able to communicate with other TP-PMD compliant systems. Receiving units would ignore any signal with an amplitude greater than the TP-PMD specified maximum.

A different set of problems characterize a design which fails to meet the minimum differential output voltage specification. A particularly significant symptom of this condition is the inability to establish communication with receive partners at the end of long cables (for example, 100 meters).

Verify that the appropriate component values have been used to implement the voltage reference component. This involves revisiting resistor and diode values for an external voltage reference or a resistor value for an internal voltage reference. The 10 and 100 Mbit biasing resistors should be verified against the values provided on reference designs. These biasing resistors should be tuned.

G.4 Overshoot (ANSI specification 9.1.3)

Excessive overshoot can cause problems because other receivers may not be designed to compensate for large amounts of overshoot.

It is absolutely imperative that low capacitance/high bandwidth probes be used for these measurements. Probes with greater than 1 pf capacitance and/or less than 1 GHz bandwidth may show false failures.

The value of the coupling capacitor between TDP and TDN should be increased in order to decrease transmit overshoot. However, increasing the value of this capacitor will reduce the transmit return loss. Additionally, it will increase the rise and fall times. Thus, an optimal value should be found through experimentation. A valid range for this capacitor on the 82558 is from 0 pF to 20 pF, with an average value of between 7 pF and 15 pF depending on the design. The required value of this capacitor is affected by both trace and magnetics capacitance.

G.5 Amplitude Symmetry (ANSI specification 9.1.4)

Incorrect amplitude symmetry can have a couple of undesired effects. First, it can decrease the distance apart two network stations can be before performance starts to seriously degrade. Assume that the receiver can pick up a 1 V peak signal over 100 meters of spec length cable. If the signal is asymmetric as shown in the figure below, the signal will only be able to be received to 95 meters of spec length cable. Even though the negative peak is 1050 mV, the limiting factor is the positive peak which is 950 mV.

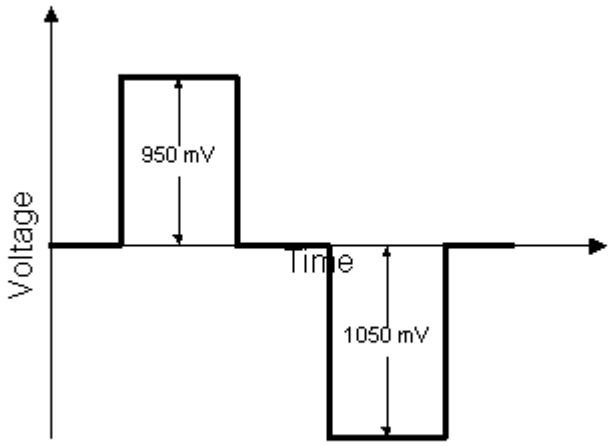

Figure G-1. Asymmetric Amplitudes

Additionally, asymmetric amplitudes could cause problems with the receiver's peak detectors, because they may be expecting both the positive and negative peaks to be at the same level. They could try to adjust the signal to make the peaks equal by adding in a DC offset, and in doing so would distort the waveform even more (because the zero point would become ambiguous).

Confirm that the resistors on TDN and TDP are identical (within 1%) and that they add up to 100 ohms. Also verify that the proper reference resistor values have been used.

G.6 Return Loss (ANSI specifications 9.1.5 and 9.2.2)

A system failing to meet return loss specifications indicates that substantial power is being reflected. Reflections are typically related to an impedance mismatch between the PHY and the transmit and receive signal traces. A system failing return loss would have a high BER on long cables, short cables, or both.

Trace geometry is a key factor in determining the impedance of traces on a board, which directly affect the design requirements. The proper impedance for both the transmit and the receive traces should be verified. Many design tools will miscalculate board parameters which affect the trace impedance. If the actual trace impedance is too low, the value can be improved by asking the board manufacturer for trace impedances higher than 100 ohms. This should provide higher impedances which are closer to 100 ohms.

If a capacitor is used between TDP and TDN to control rise time and overshoot, its value should not be too large. If the capacitance is too large, it can result in low return loss.

Trace length is also very important. Transmit and receive differential pairs should be routed at equal lengths from the PHY. The sum of all segments in one trace should be equal to the sum of all segments of its corresponding differential pair (in other words, the sum of all TDP segments equals the sum of all TDN segments). Also note that each trace in the differential pair should be run in parallel and on the same layer. Splitting the traces onto two different layers will cause poor common mode rejection.

G.7 Rise and Fall Times (ANSI specification 9.1.6)

Rise and fall times measure the time it takes for a pulse to rise to (and fall from) its peak amplitude. Slow rise and/or fall times may cause narrow pulses not to reach their maximum amplitude. Additionally, fast rise and/or fall times may increase the apparent width of the pulse and increase overshoot.

Rise and fall times are most directly affected by the capacitance between TDN and TDP, which includes both the capacitor and the trace capacitance. Increasing the capacitance increases the rise and fall times. Decreasing the capacitance will decrease the rise and fall times. This capacitance also has an impact on the transmitter return loss and overshoot. Increasing the capacitance decreases the return loss, and vice versa. Increasing the capacitance also reduces overshoot, while decreasing the capacitance increases overshoot. Experiment until a capacitance value is found that produces the best results.

G.8 Open Circuit Inductance (ANSI specification 9.1.7)

Transformers only pass AC current. If the signal being transmitted stays at ‘1’ or ‘0’ for any great length of time, it will begin to look like a DC signal to the transformer.

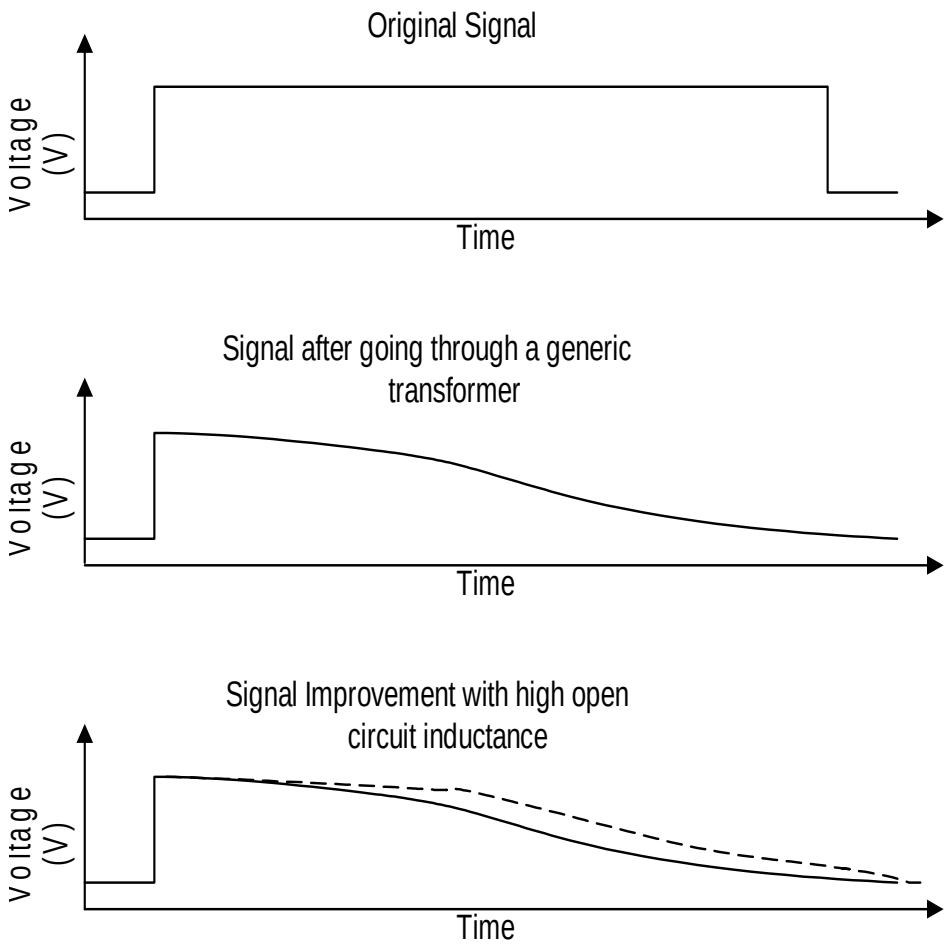

Figure G-2. Effects of low open circuit inductance for $0 \leq t \leq \infty$.

Note: The long pulse in the graphic above is meant to represent the effect of tens to hundreds of wide positive pulses in a row.

Magnetics that meet the open circuit inductance specification keep the signal quality from degrading as quickly. Systems that fail this specification may have poor BER results over long cables depending on the ability of the receiver to handle these degrading signals. Fortunately, these types of signals are never as long as shown above, so the problem will not usually be so dramatic that all of the packets will disappear. Normally, the extra inductance in the magnetics will improve the signals enough to prevent the majority of the errors.

G.9 Duty Cycle Distortion (ANSI specification 9.1.8)

Different receivers handle signals with duty cycle distortion differently. The general symptom of this problem will be that the receiver may drop some bits or it may think some bits are present when they really are not. This problem can be aggravated on a longer cable.

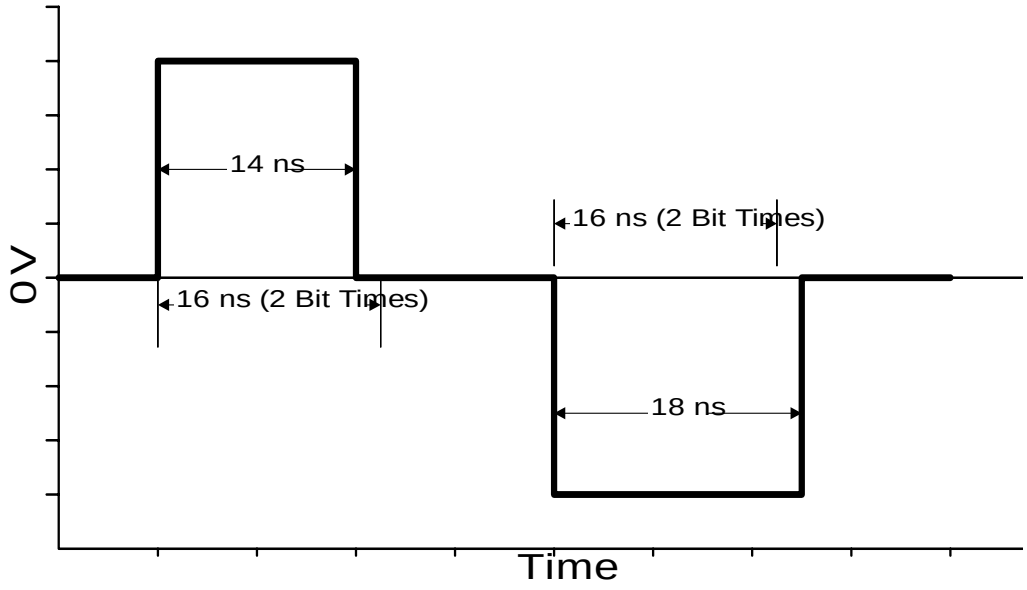

Figure G-3. Possible problems arising from duty cycle distortion. Each pulse above is meant to be two bit times.

Figure G-3 gives an idea of what could happen. Depending on the algorithm the receiver uses to detect the signal levels each bit time, it may decide that the first pulse above is only 1 bit instead of 2, and/or it may decide that the negative pulse is 3 bits instead of two. Thus, problems may only appear when transmitting to certain receive partners (with different Phy's).

If a crystal is being used, check that the loading capacitors are correct and are of equal values.

G.10 Transmit Jitter (ANSI specification 9.1.9)

Transmit jitter causes problems for the receiving unit because it becomes more difficult to distinguish the value of bits as jitter increases. Systems with excessive jitter will therefore cause the receiving unit to have high Bit Error Rates.

There are several causes of jitter that can be addressed in board design and layout. Noisy boards and poor common mode rejection will increase jitter. The noise can be made even worse by running high speed traces near the network controller or in parallel with the differential traces. To reduce noise, try as much as possible to maximize ground fill under the chip. Also make sure there is adequate decoupling between VCC and Ground around the networking chip and around other chips that may add noise to VCC. A metal top layer with several large via's down to the ground plane can reduce the problem.

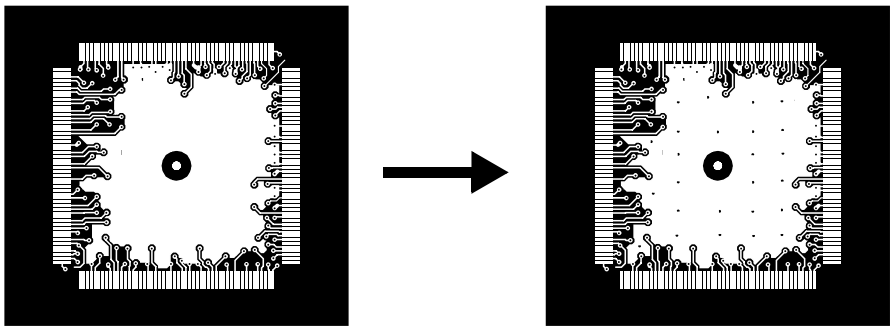

Figure G-4. Reducing jitter by reducing noise under the network controller.

Poor common mode rejection can be caused by asymmetric traces. They should be the same length, and should run parallel to each other from end to end.

Jitter can also be caused by a crystal or oscillator that is not producing the required output frequency.

G.11 Differential Input Signals (ANSI specification 9.2.1)

Bit error rate testing provides some of the most important test data. It is the data that can be most readily seen by customers. If the board is incapable of receiving without large numbers of errors, it will result in poor network performance.

Poor performance on this test can be caused by receiver circuit asymmetry or poor impedance matching as well as failure on any of the other tests in this document. Make sure that the transmitting unit is a known good unit. For example, don't use two systems with new designs to perform Bit Error tests, since any problems with the transmitter on one unit will cause the receiver to have high BER.

G.12 Receiver Common Mode Rejection (ANSI specification 9.2.3)

Common mode noise is noise which affects both wires in the differential pair simultaneously and in phase. Because it is the same across the pair, it can be rejected by the receive unit. The TP-PMD spec defines that the receiver should be able to withstand a 1 V peak-to-peak sine wave with frequencies between 0 – 125 MHz. This simulates common mode noise that could be picked up from running cables near power or telephony wiring.

For systems failing to meet common mode rejection specifications, verify that the common mode choke functionality of the magnetics module has been properly implemented. Make sure the ground planes and power planes under the magnetics module are separated by at least one-tenth of an inch between the PHY side of the magnetics module and the chassis side. Usually, this prevents common mode noise from bypassing the common mode chokes that are internal to the magnetics module.

Verify the following for both of the differential pairs (TDP and TDN, RDP and RDN) from the PHY to the magnetics module:

- Each trace is the same length.
- Each trace is the same impedance.

- One trace should mirror the other within the maximum suggested separation of one-tenth of an inch.
- Each trace needs to encounter common (or shared) components at the same distance from the PHY as the other trace in the same differential pair.

Good power to ground decoupling is important around the PHY and out to the RJ-45 connector. There are two types of decoupling capacitors, high frequency and bulk. The high frequency decoupling capacitors usually have a value of 0.1 mF and are placed throughout the board, especially close to power, ground, and fast switching signals. The bulk capacitors are used to keep the VCC and ground from bouncing. These are typically 22 mF tantalum capacitors on motherboards. However, for the family of Intel® EtherExpress™ PRO/100 adapters 4.7 mF ceramic capacitors are used.

Appendix H Summary Table of 100Base-TX Results

Section	ANSI	Characteristic	Spec Min / Max	Actual
2	9.1.2.2	Diff. signal UTP, 0V to $+V_{out}$	+950 mV to +1050 mV	mV
2	9.1.2.2	Diff. signal UTP, 0V to $-V_{out}$	-950 mV to -1050 mV	mV
3	9.1.3	Overshoot voltage, positive (Max)	Max = 5% +Vout	mV %
3	9.1.3	Overshoot voltage, negative (Max)	Max = 5% of -Vout	mV %
3	9.1.3	Overshoot settling time within 1%	Max = 8.0 nsec	ns
4	9.1.4	Signal amplitude symmetry	Ratio = 0.98 to 1.02	
5	9.1.5	TX return loss (2 MHz-30 MHz)	Min > 16 dB	N/A
5	9.1.5	TX return loss (30 MHz-60 MHz)	> 16-20log(f/30 MHz) dB	N/A
5	9.1.5	TX return loss (60 MHz-80 MHz)	Min > 10 dB	N/A
6	9.1.6	Rise time	3.0 nsec to 5.0 nsec.	ns
6	9.1.6	Fall time	3.0 nsec to 5.0 nsec.	ns
6	9.1.6	Rise and fall time symmetry	≤ 0.5 nsec.	ns
7	9.1.7	Open circuit inductance (OCL)	Min = 350µH at 0 - 8 mA	µH
8	9.1.8	Duty cycle distortion ,pk/pk	16.0 nsec ± 0.25 nsec (15.50 ns - 16.50 ns)	pos. mid. neg.
9	9.1.9	Transmit jitter	Max = 0 to 1.4 nsec	nsec
10	9.2.1	Differential Input Signals (BER) Test Cables 1-5	Max ≤ 10^{-8} BER	BER
11	9.2.2	RX return loss (2 MHz-30 MHz)	Min > 16 dB	dB
11	9.2.2	RX return loss (30 MHz-60 MHz)	> 16-20log(f/30 MHz) dB	dB
11	9.2.2	RX return loss (60 MHz-80 MHz)	Min > 10 dB.	dB
12	9.2.3	Common mode rejection (Ecm = 1 Vp-p, 100 kHz - 125 MHz)	Max ≤ 10^{-8} BER	BER

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Appendix I Summary Table of 10Base-T Results

Section	IEEE	Characteristic	Spec Min / Max	Actual	Pass / Fail
13	14.3.1.2.1	Peak differential output voltage on TD	2.2V to 2.8V pk		
14	14.3.1.2.1	Harmonic content, all ones signal	27 dB below F_0		
15	14.3.1.2.2	TD circuit differential output impedance	15 dB below incident		
16	14.3.1.2.5	TD circuit common-mode output voltage	Max = 50 mV pk		
17	14.3.1.2.3	Transmitter output timing jitter with cable model	See specification		
18	14.3.1.2.3	Transmitter output timing jitter without cable model	See specification		
19		RD Receiver Circuit Signal Acceptance Test (BER)	$<1x10^{-8}$		
20	14.3.1.3.4	RD circuit differential input impedance	15 dB below incident		

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Appendix J Pattern File

The following is the 000880.pat pattern file used with the test software.

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00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00
08 80

00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00 08 80

00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00 08 80 00 08 80
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